Evaluation board for AEM30940 - RF harvesting

Description

The AEM30940 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM30940 integrated circuit (IC). Please refer to the datasheet for all the useful details about the AEM30940 (Document DS_AEM30940).

The AEM30940 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting. It includes six matching networks and rectifiers for a 50 Ω single-ended antenna. It allows easy connections to the RF energy harvester, the storage element and the low-voltage and high-voltage loads. It also provides all the configuration access to set the device in configuration modes described in the datasheet. The MPPT ratio is fixed at 50% to optimize the rectifier efficiency. The control and status signals are available on standard pin headers, allowing users to wire for any usage scenario and evaluate the relevant performance.

The AEM30940 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes) for the design of a highly efficient radio frequency powered subsystem in your target application.

Applications

- RF harvesting
- Industrial monitoring
- Indoor geolocation
- Home automation
- E-health monitoring
- Wireless sensor nodes

Features

Three two-way screw terminals
- Low-voltage load
- High-voltage load
- Primary energy storage element

One three-way screw terminal
- Energy storage element (battery or (super)capacitor)

Six male 50 Ω SMA connectors
- Connections to the RF source
- Associated matching networks and rectifiers

One 2-pin "Shrouded Header"
- Alternative connection for the storage element

Six 3-pin headers
- Low drop-out regulators (LDOs) enabling
- Energy storage elements and LDOs configuration
- Dual-cell supercapacitor configuration

Height 2-pin headers
- Primary battery configuration
- Connection from rectifier to AEM30940

Provision for height resistors
- Custom mode configuration
- Primary battery configuration

Three 1-pin headers
- Access to status pins

Device information

<table>
<thead>
<tr>
<th>Part number</th>
<th>Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>2AEM30940C0111</td>
<td>79 mm x 61 mm</td>
</tr>
</tbody>
</table>

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1 Connections Diagram

**Warning**
- Please refer to Section 2.1 before doing any connection
- A 150 µF capacitor CBATT is already soldered on BATT

**High-voltage LDO output**
- Leave floating if not used

**Low-voltage LDO output**
- Leave floating if not used

**Custom mode configuration**
- Leave floating if not used
- See Section 2.3.1

**Storage element**
- Mandatory connection
- BAL (paralleled line) signal
- Connect the jumper «BAL» to «ToCN» if BAL pin used or to «GND» if not used
- See Section 2.3.3

**Primary battery**
- Mandatory connection
- Connect a jumper to each «NoPRIM» 2-pins or connect the battery
- See Section 2.3.2

**Battery & LDOs configuration**
- Mandatory connection
- See Table 2

**Frequency selection**
- Leave floating if not used
- See Table 4

**Source element**
- Leave floating if not used
- See Table 4
## 1.1 Signals description

<table>
<thead>
<tr>
<th>NAME</th>
<th>FUNCTION</th>
<th>CONNECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power signals</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LOUT</td>
<td>Output of the low-voltage LDO regulator.</td>
<td>Connect a load.</td>
</tr>
<tr>
<td>HVOUT</td>
<td>Output of the high-voltage LDO regulator.</td>
<td>Connect a load.</td>
</tr>
<tr>
<td>BAL</td>
<td>Connection to mid-point of a dual-cell supercapacitor.</td>
<td>Connect mid-point and jumper BAL to &quot;ToCN&quot;.</td>
</tr>
<tr>
<td>BATT</td>
<td>Connection to the energy storage element.</td>
<td>Connect storage element in addition to CBATT (150μF).</td>
</tr>
<tr>
<td>PRIM</td>
<td>Connection to the primary battery.</td>
<td>Connect primary battery.</td>
</tr>
<tr>
<td><strong>Debug signals</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VBOOST</td>
<td>Output of the boost converter.</td>
<td></td>
</tr>
<tr>
<td>VBUCK</td>
<td>Output of the buck converter.</td>
<td></td>
</tr>
<tr>
<td>SRC</td>
<td>Output of the rectifier</td>
<td></td>
</tr>
<tr>
<td><strong>Configuration signals</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CFG[2]</td>
<td>Configuration of the threshold voltages for the energy storage element and the output voltage of the LDOs.</td>
<td>Connect jumper (see Table 2).</td>
</tr>
<tr>
<td>CFG[1]</td>
<td></td>
<td>Cannot be left floating (see Table 2).</td>
</tr>
<tr>
<td>CFG[0]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BAND 1</td>
<td>Selection of the 863 MHz - 868 MHz band.</td>
<td>Connect jumper (see Table 2).</td>
</tr>
<tr>
<td>BAND 2</td>
<td>Selection of the 915 MHz - 921 MHz band.</td>
<td>Leave floating.</td>
</tr>
<tr>
<td>BAND 3</td>
<td>Selection of the 925 MHz - 960 MHz band.</td>
<td></td>
</tr>
<tr>
<td>BAND 4</td>
<td>Selection of the 1805 MHz - 1880 MHz band.</td>
<td></td>
</tr>
<tr>
<td>BAND 5</td>
<td>Selection of the 2110 MHz - 2170 MHz band.</td>
<td></td>
</tr>
<tr>
<td>BAND 6</td>
<td>Selection of the 2400 MHz - 2500 MHz band.</td>
<td></td>
</tr>
<tr>
<td>FBPRIM</td>
<td>Configuration of the primary battery.</td>
<td>Use resistors R7-R8 (see Section 2.3.3). Connect a jumper to each NoPRIM 2-pins.</td>
</tr>
<tr>
<td>FBJHV</td>
<td>Configuration of the high-voltage LDO in the custom mode.</td>
<td>Use resistors R5-R6 (see Section 2.3.1). Leave floating.</td>
</tr>
<tr>
<td>RZMPP</td>
<td>Unused</td>
<td></td>
</tr>
<tr>
<td><strong>Control signals</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENHV</td>
<td>Enabling pin for the high-voltage LDO.</td>
<td>Connect jumper (see Table 3).</td>
</tr>
<tr>
<td>ENLV</td>
<td>Enabling pin for the low-voltage LDO.</td>
<td>Connect jumper (see Table 3).</td>
</tr>
<tr>
<td><strong>Status signals</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS[2]</td>
<td>Logic output. Asserted when the AEM performs the MPP evaluation.</td>
<td></td>
</tr>
<tr>
<td>STATUS[1]</td>
<td>Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.</td>
<td></td>
</tr>
<tr>
<td>STATUS[0]</td>
<td>Logic output. Asserted when the LDOs can be enabled.</td>
<td></td>
</tr>
</tbody>
</table>

*Table 1: Pin description*
2 General Considerations

2.1 Safety information

Always connect the elements in the following order:

1. Reset the board - see “How to reset the AEM30940 evaluation board” on page 7.

2. Completely configure the PCB (jumpers/resistors);
   - Frequency band selection - see Table 4,
   - Battery and LDOs configuration (CFG[0], CFG[1], CFG[2] and, if needed, R1-R2-R3-R4-R5-R6) - see Table 2,
   - Primary battery configuration (NoPRIM or R7-R8) - see Section 2.3.3,
   - LDOs enabling (ENHV and ENLV) - see Table 3,
   - Balun circuit connection (BAL) - see Section 2.3.4.

3. Connect the storage elements on BATT and optionally the primary battery on PRIM.

4. Connect the high and/or low voltage loads on HVOUT/LVOUT (optional).

5. Connect the source.

To avoid damage to the board, users are urged to follow this procedure.

2.2 Basic configurations

The MPP configuration is not available on the AEM30940 evaluation board. The MPP is by default configured to 50% of \(V_{oc}\) as this ratio optimize the proposed rectifier efficiency.

<table>
<thead>
<tr>
<th>Configuration pins</th>
<th>Storage element threshold voltages</th>
<th>LDOs output voltages</th>
<th>Typical use</th>
</tr>
</thead>
<tbody>
<tr>
<td>H       H       H</td>
<td>4.12 V</td>
<td>3.67 V</td>
<td>3.60 V</td>
</tr>
<tr>
<td>H       H       L</td>
<td>4.12 V</td>
<td>4.04 V</td>
<td>3.60 V</td>
</tr>
<tr>
<td>H       L       H</td>
<td>4.12 V</td>
<td>3.67 V</td>
<td>3.01 V</td>
</tr>
<tr>
<td>H       H       L</td>
<td>2.70 V</td>
<td>2.30 V</td>
<td>2.20 V</td>
</tr>
<tr>
<td>L       H       H</td>
<td>4.50 V</td>
<td>3.67 V</td>
<td>2.80 V</td>
</tr>
<tr>
<td>L       H       L</td>
<td>4.50 V</td>
<td>3.92 V</td>
<td>3.60 V</td>
</tr>
<tr>
<td>L       L       H</td>
<td>3.63 V</td>
<td>3.10 V</td>
<td>2.80 V</td>
</tr>
<tr>
<td>L       L       L</td>
<td>4.50 V</td>
<td>3.67 V</td>
<td>2.80 V</td>
</tr>
</tbody>
</table>

Table 2: Usage of CFG[2:0]

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Frequency band [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAND 1</td>
<td>863 - 868</td>
</tr>
<tr>
<td>BAND 2</td>
<td>915 - 921</td>
</tr>
<tr>
<td>BAND 3</td>
<td>925 - 960</td>
</tr>
<tr>
<td>BAND 4</td>
<td>1805 - 1880</td>
</tr>
<tr>
<td>BAND 5</td>
<td>2110 - 2170</td>
</tr>
<tr>
<td>BAND 6</td>
<td>2400 - 2500</td>
</tr>
</tbody>
</table>

Table 4: Available frequency bands

<table>
<thead>
<tr>
<th>ENLV</th>
<th>ENHV</th>
<th>LV output</th>
<th>HV output</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>Enabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>Enabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>Disabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

Table 3: LDOs enabling
2.3 Advanced configurations

A complete description of the system constraints and configurations is available in Section 8 “System configuration” of the AEM30940 datasheet. A reminder on how to compute the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found at the e-peas website.

2.3.1 Custom mode

In addition to the pre-defined protection levels, the custom mode allows users to define their own levels via resistors R1 to R4 and to tune the output of the high voltage LDO via resistors R5-R6.

By defining \( RT = R1 + R2 + R3 + R4 \) (1 MΩ ≤ \( RT \) ≤ 100 MΩ):
- \( R1 = RT \left( \frac{1\,\text{V}}{V_{ovch}} \right) \)
- \( R2 = RT \left( \frac{1\,\text{V}}{V_{chrdy}} - \frac{1\,\text{V}}{V_{ovch}} \right) \)
- \( R3 = RT \left( \frac{1\,\text{V}}{V_{ovdis}} - \frac{1\,\text{V}}{V_{chrdy}} \right) \)
- \( R4 = RT \left( 1 - \frac{1\,\text{V}}{V_{ovdis}} \right) \)

By defining \( RV = R5 + R6 \) (1 MΩ ≤ \( RV \) ≤ 40 MΩ):
- \( R5 = RV \left( \frac{1\,\text{V}}{V_{hv}} \right) \)
- \( R6 = RV \left( 1 - \frac{1\,\text{V}}{V_{hv}} \right) \)

Make sure the protection levels satisfy the following conditions:
- \( V_{chrdy} + 0.05\,\text{V} \leq V_{ovch} \leq 4.5\,\text{V} \)
- \( V_{ovdis} + 0.05\,\text{V} \leq V_{chrdy} \leq V_{ovch} - 0.05\,\text{V} \)
- \( 2.2\,\text{V} \leq V_{ovdis} \)
- \( V_{hv} \leq V_{ovdis} - 0.3\,\text{V} \)

If unused, leave the resistor footprints (R1 to R6) empty.

2.3.2 ZMPP configuration

If this configuration is chosen (see ??), the AEM30940 regulate \( V_{src} \) at a voltage equals to the product of R1 times the current available at the output of the internal rectifier.

- \( 10\,\Omega \leq R_{ZMPP} \leq 1\,\text{MΩ} \)

If unused, leave the resistor footprint R1 empty.

2.3.3 Primary battery configuration

As to the main storage element, the primary battery protection levels have to be defined. To do so, use resistors R7-R8.

By defining \( RP = R7 + R8 \) (100 kΩ ≤ \( RP \) ≤ 500 kΩ):
- \( R7 = \left( \frac{V_{prim_{min}}}{4} \right) \times RP \)
- \( R8 = RP - R7 \)

If unused, connect a jumper to each “NoPRIM” 2-pins.

2.3.4 Balun circuit configuration

When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balun circuit configuration to ensure equal voltage on both cells. To do so:
- Connect the node between the two supercapacitor cells to BAL (on BATT connector)
- Use a jumper to connect “BAL” to “ToCN”

If unused, use a jumper to connect ”BAL” to ”GND”.

- Vhv ≤ Vovdis - 0.3 V

If unused, leave the resistor footprints (R1 to R6) empty.
How to reset the AEM30940 evaluation board:
To reset the board, simply disconnect the storage device and the optional primary battery and connect the 6 "Reset" connections (working from the rightmost to the left) to a GND node (i.e. the negative pin of any connector) in order to discharge the internal nodes of the system.

3 Functional Tests
This section presents a few simple tests that allow the user to understand the functional behavior of the AEM30940. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results.

The following functional tests were made using the following setup:
- Configuration: CFG[2:0] = HLL, BAND 1 connected, ENLV = H, ENHV = H
- Storage element: capacitor (4.7 mF + CBATT)
- Load: 10 kΩ on HVOUT, LVOUT floating
- SRC: current source (1 mA or 100 μA) with voltage compliance (4 V)

Feel free to adapt the setup to match your system as long as you respect the input and cold-start constraints (see Section 1 “Introduction” of AEM30940 datasheet).

3.1 Start-up
The following example allows users to observe the behavior of the AEM30940 in the wake-up mode.

Setup
1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1.

Observations and measurements
- BATT: Voltage rises as the power provided by the source is transferred to the storage element (see Figure 2).
- HLDO/LLDO: Regulated when voltage on BATT first rises above Vchrdy (see Figure 2).
- STATUS[0]: Asserted when the LDOs are ready to be enabled (refer to Section 7.2 “Normal mode” of the AEM30940 datasheet) (see Figure 2).

3.2 Shutdown
This test allows users to observe the behavior of the AEM30940 when the system is running out of energy.
**Setup**

1. Place the probes on the nodes to be observed.

2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1. Configure the board in the desired state and start the system (see Section 3.1). Do not use a primary battery.

3. Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).

4. Remove your source element and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

**Observations and measurements**

- **BATT**: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage remains stable after crossing Vovdis (see Figure 4).

- **STATUS[0]**: De-asserted when the LDOs are no longer available as the storage element is running out of energy. This happens 600 ms after STATUS[1] assertion (see Figure 4).

- **STATUS[1]**: Asserted for 600 ms when the storage element voltage (BATT) falls below Vovdis (see Figure 4).

**3.3 Switching on primary battery**

This example allows users to observe switching from the main storage element to the primary battery when the system is running out of energy.

**Setup**

1. Place the probes on the nodes to be observed.

2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1. Configure the board in the desired state and start the system (see Section 3.1). Connect a primary battery (example: 3.1 V coin cell with protection level at 2.4 V, R7 = 68 kΩ and R8 = 180 kΩ).

3. Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).

4. Remove your source element and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

**Observations and measurements**

- **BATT**: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches Vovdis and then rises again to Vchrdy as it is recharged from the primary battery (see Figure 5).

- **STATUS[0]**: Never de-asserted as the LDOs are still functional (see Figure 5).

- **HLDO**: Stable and not affected by switching on the primary battery (see Figure 5).

**Figure 5: Switching from SRC to the primary battery**

**3.4 Cold start**

The following test allows users to observe the minimum voltage required at SRC to coldstart the AEM30940. Be careful to avoid probing any unnecessary node to avoid leakage current induced by the probe. Make sure to properly reset the board to observe the cold-start behavior.

**Setup**

1. Place the probes on the nodes to be observed.

2. Referring Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Do not plug any storage element in addition to CBATT.

3. SMA connector: Connect your source element.
Observation and measurements

- **SRC**: Equal to the cold-start voltage during the cold-start phase. Regulated at the selected MPPT percentage of $V_{oc}$ when cold start is over (see Figure 6). Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.

- **BATT**: Starts to charge when the cold-start phase is over (see Figure 6).

![Figure 6: AEM30940 behaviour during cold start](image)

3.5 Dual-cell supercapacitor balancing circuit

This test allows users to observe the balancing circuit behavior that maintains the voltage on BAL equilibrated.

**Setup**

1. Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state. Plug the jumper linking "BAL" to "ToCN".

2. **BATT**: Plug capacitor C1 between the positive (+) and the BAL pins and a capacitor C2 between BAL and the negative (-) pins. Select $C_1 \neq C_2$ such that:
   
   - $C_1 \times V_{chrdy} \geq 0.9 \text{ V}$
   
3. SMA connector: Plug your source element to start the flow of power to the system.

**Measurements**

- **BAL**: Equal to half the voltage on **BATT**.
4 Performance Tests

This section presents the tests to reproduce the performance graphs found in the AEM30940 datasheet and to understand the functionalities of the AEM30940. To be able to reproduce those tests, you will need the following:
- 1 voltage source
- 2 source measure units (SMUs)
- 1 oscilloscope

To avoid damaging the board, follow the procedure found in Section 2.1 “Safety information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results (see "How to reset the AEM30940 evaluation board" on page 7).

4.1 LDOs

The following example instructs users on how to measure the output voltage stability of the LDOs (Figure 16 and Figure 17 of AEM30940 datasheet).

Setup

1. Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state and plug your storage element(s).

2. **VBOOST**: Connect SMU1. Configure it to source voltage with a current compliance of 200 mA.

3. **HVOUT / LVOUT**: Connect SMU2 to the LDO you want to measure. Configure it to sink current with a compliance of 5 V for HVOUT or 2.5 V for LVOUT.

Manipulations

1. Impose a voltage between Vovch and 5 V on SMU1 to force the AEM to start.

2. Sweep voltage on SMU1 from Vovdis + 50 mV to 4.5 V.

3. Repeat with different current levels on SMU2 (from 10 µA to 80 mA for HVOUT and from 10 µA to 20 mA for LVOUT).

Measurements

- **HVOUT/LVOUT**: Measure the voltage.

4.2 BOOST efficiency

This test allows users to reproduce the efficiency graphs of the boost converter (Figure 14 of AEM30940 datasheet).

Setup

1. Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state.

2. **VBUCK**: Connect a 2.3 V voltage source to prevent VBUCK to sink from VBOOST.

3. **SRC**: Connect SMU1. Configure it to source current with a voltage compliance of 0 V.

4. **VBOOST**: Connect SMU2. Configure it to source voltage with a current compliance of 200 mA.

5. **STATUS[2]**: Connect to one of the SMUs to detect falling edge.

Manipulations

1. Impose a voltage between Vchrdy and 5 V on SMU2 to force the AEM to start. When done, impose a voltage between Vovdis + 50 mV and Vovch.

2. Sweep voltage compliance on SMU1 from 50 mV to 5 V.

3. Repeat with different current levels on SMU1 (from 100 µA to 100 mA) and with different voltage levels on SMU2 (from Vovdis + 50 mV to Vovch).

Measurements

- **STATUS[2]**: Do not make any measurements while high (boost converter is not active during MPP calculation).
- **SRC**: Measure the current and the voltage.
- **VBOOST**: Measure the current and the voltage. Repeat the measurement a copious number of times to be sure to capture the current peaks. Figure 8 has been obtained by averaging over 100 measurements configured with a 100 ms integration time.

- Deduce input and output power \( P = U \times I \) and efficiency \( \eta = \frac{P_{out}}{P_{in}} \).

**Figure 8**: Boost efficiency for ISRC = 1 mA

### 4.3 Custom mode configuration

This test allows users to measure the custom protection levels of the storage element set by resistors R1 to R6.

**Setup**

1. Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Connect CFG[2:0] = LLL to select custom mode and choose R1 to R6 to configure the battery protection levels and HVOUT output voltage.

2. Place the probes on the nodes to be observed.

3. SMA connector: Connect your source element to start the flow of power to the system.

**Manipulations**

1. Shut down the source element after the voltage on BATT has reached steady state (between Vchrdy and Vovch).

**Measurements**

Measure the following nodes to ensure the correct behaviour of the AEM30940 with respect to the custom configuration:

- **STATUS[0]**: Asserted when the LDOs can be enabled (i.e. when BATT first rises above Vchrdy).

- **STATUS[1]**: Asserted when BATT falls below Vovdis.

- **BATT**: Rise up and oscillate around Vovch as long as the source element has not been removed.

- **HVOUT**: Equal to the value set by R5-R6.