AEM20940 Evaluation Board User Guide

Description

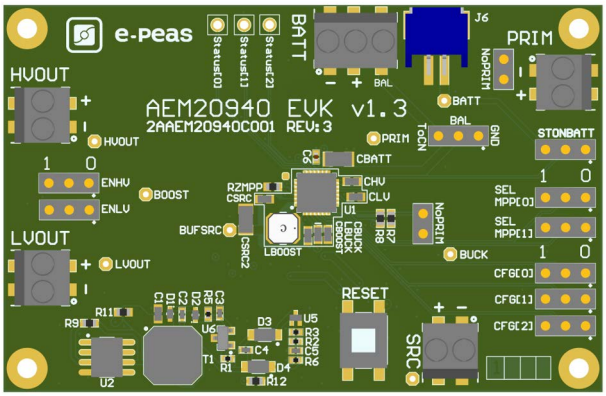
The AEM20940 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM20940 integrated circuit (IC). Please refer to the datasheet for all the useful details about the AEM20940 (Document DS_AEM20940).

The AEM20940 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting.

It allows easy connections to the TEG (Thermo Electric Generator) energy harvester, the storage element, the low-voltage and the high-voltage loads. It also provides all the configuration access to set the device in any one of the modes described in the datasheet. The control and status signals are available on standard pin headers, allowing users to wire for any usage scenario and evaluate the relevant performance.

The AEM20940 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes…) for the design of a highly efficient subsystem powered by TEG energy harvesting in your target application.

Appearance



Features

Two-way screw terminals

- Source of energy (TEG).
- Low-voltage load.
- High-voltage load.
- Primary energy storage element.
- Resistor for ZMPP configuration.

Three-way screw terminals

- Energy storage element (Battery or (super)capacitor).

2-pin “Shrouded Header”

- Alternative connection for the storage element.

3-pin headers

- Maximum power point tracker (MPPT) configuration.
- Low drop-out regulators (LDOs) enabling.
- Energy storage elements and LDOs configuration.
- Dual-cell supercapacitor configuration.
- Start-on-battery configuration.

2-pin headers

- Primary battery configuration.

Provision for resistors

- Primary battery configuration.
- ZMPP configuration.

1-pin headers

- Access to status pins.

EvB Information

Part Number	Dimensions
2AAEM20940C001 REV:3	76 mm x 49 mm

Device Information

Part Number	Dimensions
10AEM20940C0010	5 mm x 5 mm

1. Connections Diagram

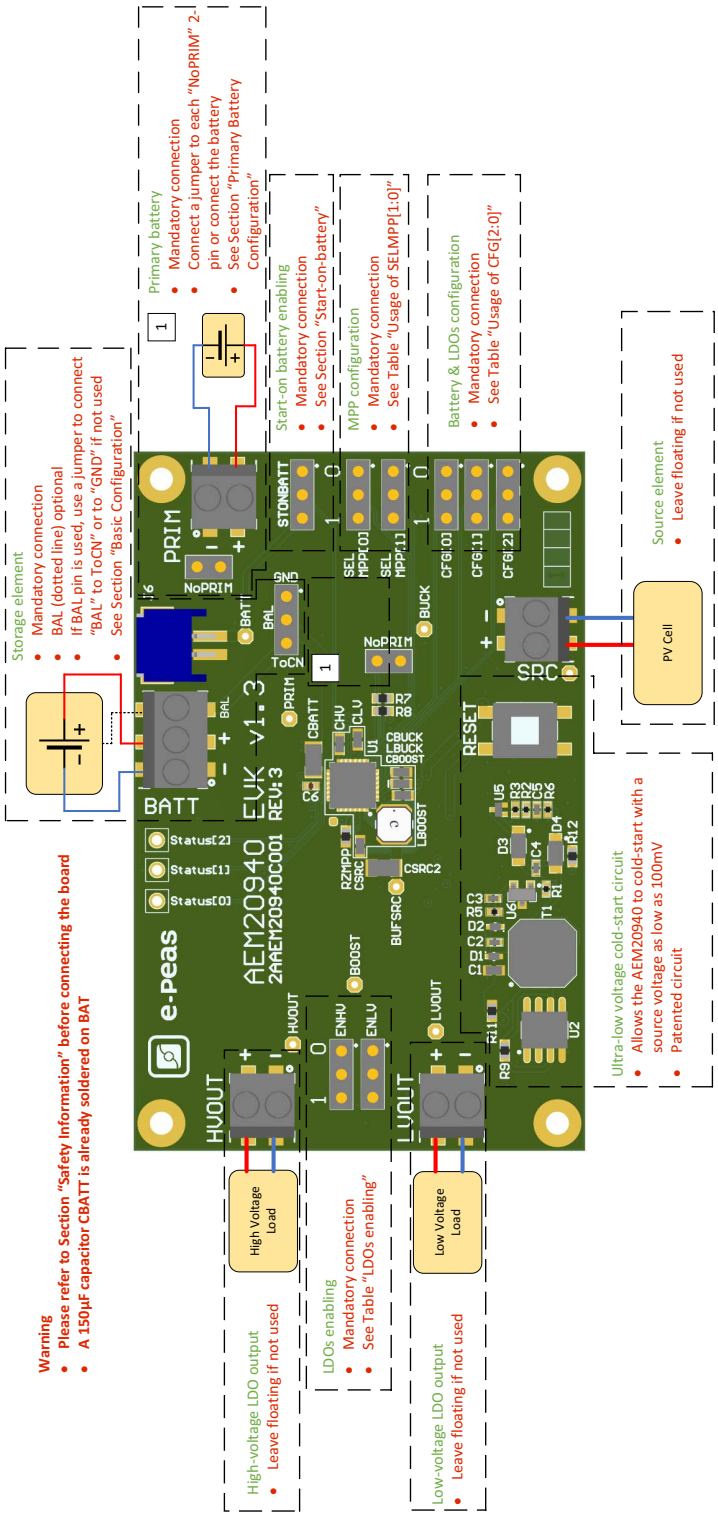


Figure 1: Connection Diagram

1.1. Signals Description

		If used	If not used
NAME	**FUNCTION**	**CONNECTION**	
Power signals			
SRC	Connection to the harvested energy source.	Connect the source element.	
BATT	Connection to the energy storage element.	Connect the storage element in addition to CBATT[a] (min 150 µF).	Do not remove CBATT.
BAL	Connection to mid-point of a dual-cell supercapacitor.	Connect mid-point of supercapacitor and a jumper from “BAL” to “ToCN”.	Use a jumper to connect “BAL” to “GND”.
PRIM	Connection to the primary battery.	Connect primary battery and remove the “NoPRIM” jumpers.	Connect a jumper to each “NoPRIM” 2-pin.
LVOUT	Output of the low-voltage LDO regulator.	Connect a load.	Leave floating
HVOUT	Output of the high-voltage LDO regulator.	Connect a load.	Leave floating
Debug signals			
VBOOST	Output of the boost converter.		
VBUCK	Output of the buck converter.		
BUFSRC	Connection to an external capacitor buffering the boost converter input.		
Configuration signals			
CFG[2:0]	Configuration of the threshold voltages for the energy storage element.	Connect jumpers (see Table 2).	Cannot be left floating (see Table 2).
SELMPP[1:0]	Configuration of the MPP ratio.	Connect jumpers (see Table 4).	Cannot be left floating (see Table 4).
FB_PRIM_D FB_PRIM_U	Configuration of the primary battery.	Use resistors R7-R8 (see Section 2.3.3).	Connect a jumper to each “NoPRIM” 2-pin.
RZMPP	Configuration of the constant impedance ZMPP.	Use resistor RZMPP (see Section 2.3.1).	Leave floating.
STONBAT	Configuration of the start on BAT feature.	Connect jumper to “1” (see Section 2.3.2).	Connect jumper to “0” (see Section ???).
Control signals			
ENHV	Enabling pin for the high-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating (see Table 3).
ENLV	Enabling pin for the low-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating (see Table 3).
Status signals			
STATUS[2]	Logic output. Asserted when the AEM performs a MPP evaluation.		
STATUS[1]	Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.		
STATUS[0]	Logic output. Asserted when the LDOs can be enabled.		

Table 1: Pin Description

a.CBATT capacity on the EvK may vary depending on suppliers availability, with a minimum value of 150µF.

2. General Considerations

2.1. Safety Information

Always connect the elements in the following order:

1. Reset the board - see “How to reset the AEM20940 evaluation board” on Figure 2.
2. Completely configure the PCB (jumpers/resistors):
   - MPP configuration (SELMPP[1:0], RZMPP) - see Table 4.
   - Battery and LDOs configuration (CFG[2:0]) - see Table 2.
   - Primary battery configuration (“NoPRIM” or R7-R8) - see Section 2.3.3.
   - LDOs enabling (ENHV and ENLV) - see Table 3.
   - Balancing circuit connection (BAL) - see Section 2.3.4.
3. Connect the storage elements on BATT and optionally the primary battery on PRIM.
4. Connect the high and/or low voltage loads on HVOUT/LVOUT (optional).
5. Connect the on SRC.

To avoid damage to the board, users are urged to follow this procedure.

How to reset the AEM20940 evaluation board:

To reset the board, simply disconnect the storage element and the optional primary battery and press the reset button in order to discharge the internal nodes of the system.

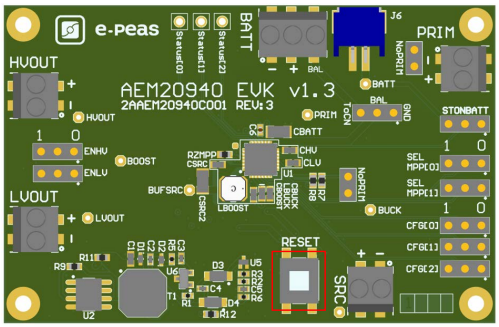


Figure 2: Board Reset

2.2. Basic Configurations

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Reserved for future use.					

Table 2: Usage of CFG[2:0]

ENLV	ENHV	LV output	HV output
H	H	Enabled	Enabled
H	L	Enabled	Disabled
L	H	Disabled	Enabled
L	L	Disabled	Disabled

Table 3: LDOs enabling

SELMPP[1]	SELMPP[0]	Vmpp/Voc
L	L	50%
L	H	55%
H	L	75%
H	H	ZMPP

Table 4: Usage of SELMPP[1:0]

2.3. Advanced Configurations

A complete description of the system constraints and configurations is available in the AEM20940 datasheet "System configuration" Section.

A reminder on how to calculate the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found on e-peas website.

2.3.1. ZMPP Configuration

If this configuration is chosen (see Table 4), the AEM20940 regulates V_{SRC} at a voltage equals to the product of R_{ZMPP} times the current available at the source.

If unused, leave the resistor footprint R_{ZMPP} empty.

2.3.2. Start-on-battery

This functionality allows to start the system on a pre-charged storage element and therefore to avoid the cold-start constraints. To use this functionality, use a jumper to connect "STONBATT" to "1" and a storage element on BATT. The storage element must be charged to a voltage higher than V_{CHRDY}.

If unused, use a jumper to connect "STONBATT" to "0".

2.3.3. Primary Battery Configuration

If a primary storage is used, it is mandatory to determine $V_{PRIM,MIN}$, the voltage at which the primary battery is considered fully depleted. To do so, use resistors R7 - R8.

These resistors are calculated as follows:

- $R_P = R7 + R8$
- $100k\Omega \leq R_P \leq 500k\Omega$
- $R7 = \frac{V_{PRIM\_MIN}}{4} \cdot R_P \cdot \frac{1}{2.2V}$
- $R8 = R_P - R7$

If unused, use a jumper to short each "NoPRIM" 2-pin headers.

2.3.4. Balancing Circuit Configuration

When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balancing circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two supercapacitor cells to BAL (on BATT connector).
- Use a jumper to connect "BAL" to "ToCN".

If unused, use a jumper to connect "BAL" to "GND".

3. Functional Tests

This section presents a few simple tests that allow the user to understand the functional behavior of the AEM20940. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted make sure to properly reset the system to obtain reproducible results.

Those functional tests were made using the following setup:

- Configurations:
  - SELMPP[1:0] = LL
  - CFG[2:0] = HLL, ENHV = H, ENLV = H.
- Storage element: Capacitor (4.7 mF + CBATT).
- Loads: 4.7 kΩ on HVOUT. LVOUT left floating.
- SRC: current source (1 mA or 100 µA) with voltage compliance (4V).

Feel free to adapt the setup to match your system as long as the input and cold-start constraints are respected (see the AEM20940 datasheet “Introduction” Section).

3.1. Start-up

The following example allows users to observe the behavior of the AEM20940 in the wake-up mode.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.

Observations and Measurements

- BATT: Voltage rises as the power provided by the source is transferred to the storage element (see Figure 3).
- SRC: Regulated at V_{MPP}, which is a voltage equal to the open-circuit voltage (V_{OC}) times the MPP ratio defined in Table 4. V_{SRC} equals V_{OC} during MPP evaluation (see Figure 4). Note that Vsrc must be higher than 380 mV to coldstart.
- HVOUT/LVOUT: Regulated when voltage on BATT first rises above V_{CHRDY} (see Figure 3).
- STATUS[0]: Asserted when the LDOs are ready to be enabled (refer to the AEM20940 datasheet “Normal Mode” section) (see Figure 3).
- STATUS[2]: Asserted each time the AEM20940 performs a MPP evaluation (See Figure 4).

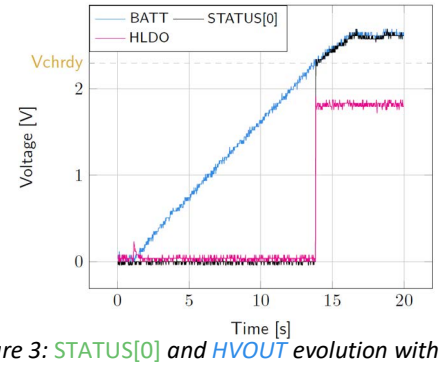


Figure 3: STATUS[0] and HVOUT evolution with BATT

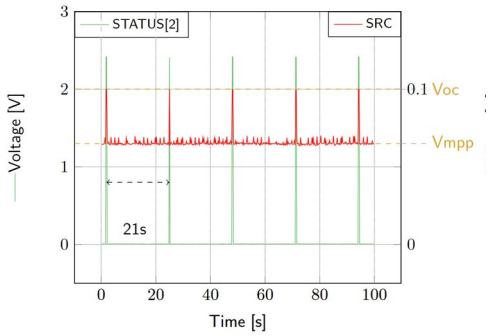


Figure 4: SRC and STATUS[2] while energy is extracted from SRC (BATT under V_{OVCH})

3.2. Shutdown

This test allows users to observe the behavior of the AEM20940 when the system is running out of energy.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1). Do not use a primary battery.
- Let the system reach a steady state (i.e. voltage on BATT between V_{CHRDY} and V_{OVCH} and STATUS[0] asserted).
- Remove the PV cell and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and Measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage remains stable after crossing V_{OVDIS} (see Figure 5).

- STATUS[0]: De-asserted when the LDOs are no longer available as the storage element is running out of energy. This happens 600 ms after STATUS[1] assertion (see Figure 5).
- STATUS[1]: Asserted for 600ms when the storage element voltage (BATT) falls below V_{OVDIS} (see Figure 5).

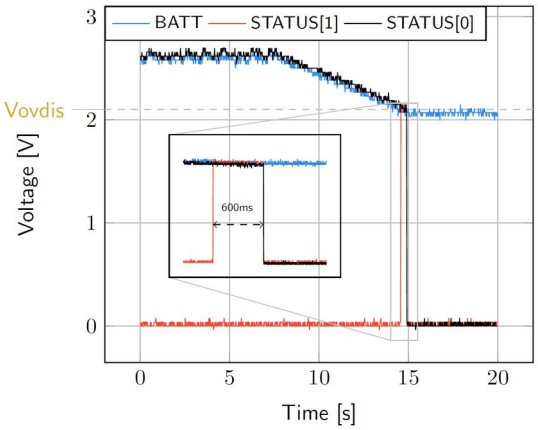


Figure 5: LDOs disabled around 600 ms after BATT reaches V_{OVDIS}

3.3. Switching on Primary Battery

This example allows users to observe switching from the main storage element to the primary battery when the system is running out of energy.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1). Connect a primary battery (example: 3.1 V coin cell with protection level at 2.4 V, R7 = 68 kΩ and R8 = 180 kΩ).
- Let the system reach a steady state (i.e. voltage on BATT between V_{CHRDY} and V_{OVDIS} and STATUS[0] asserted).
- Remove the PV cell and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and Measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches V_{OVDIS} and than rises again to V_{CHRDY} as it is recharged from the primary battery (see Figure 6).
- STATUS[0]: Never de-asserted as the LDOs are still functional (see Figure 6).
- HVOUT: Stable and not affected by switching on the primary battery (see Figure 6).

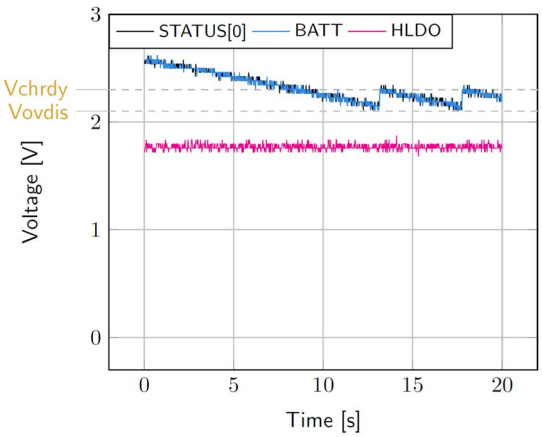


Figure 6: Switching from SRC to the primary battery

3.4. Cold Start

The following test allows the user to observe the minimum voltage required to coldstart the AEM20940. To prevent leakage current induced by the probe, the user should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behavior.

Setup

- Place the probes on the nodes to be observed.
- Referring Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Do not plug any storage element in addition to CBATT.
- SRC: Connect your source element. To match Figure 7 voltages, set the source compliance to 500mV. This is to ease differentiating the cold start voltage (about 60mV) from the MPP voltage (50% * 100 mV = 50mV).

Observations and Measurements

- SRC: Equal to the cold-start voltage during the cold-start phase. Regulated at the selected MPPT percentage of V_{OC} when cold start is over. (See Figure 7). Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.
- BATT: Starts to charge when the cold-start phase is over (see Figure 7).

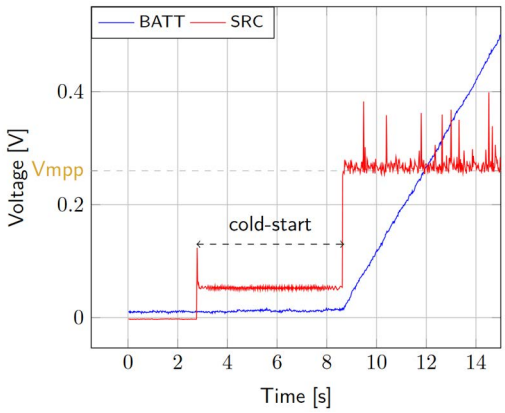


Figure 7: AEM20940 behavior during cold start

3.5. Dual-cell Supercapacitor Balancing Circuit

The following test allows the user to observe the balancing circuit behavior that balances the voltage on both side of the BAL pin.

Setup

- Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state. Plug the jumper linking "BAL" to "ToCN".
- BATT: Plug a capacitor C1 between the positive (+) pin and the BAL pin, and a capacitor C2 between the BAL pin and the negative (-) pin.
  - C1 & C2 > 1 mF.
  - (C2 x V_{CHRDY}) / C1 ≥ 0.9 V.
- SRC: Connect your source element to power up the system.

Observations and Measurements

- BAL voltage equals half of the BATT voltage.

Warning regarding measurements:

Any item connected to the PCB (load, probe, storage device, etc.) involves a leakage current. This can negatively impact the measurements. Whenever possible, disconnect unused items to limit this effect.

4. Performance Tests

This section presents the tests to reproduce the performance graphs found in the AEM20940 datasheet and to understand the functionalities of the AEM20940. To be able to reproduce those tests, the following equipment is required:

- 1 voltage source.
- 2 source measure units (SMUs).
- 1 oscilloscope.

To avoid damaging the board, follow the procedure in Section 2.1 “Safety Information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results (see “How to reset the AEM20940 evaluation board” in Section 2.1).

4.1. LDOs

The following example instructs users on how to measure the output voltage stability of the LDOs (Low-voltage and High-voltage LDO regulation Sections of the AEM20940 datasheet).

Setup

- Referring to Figure 1, follow steps 1 and 2 explained in the Section 2.1. Configure the board in the desired state and connect your storage element(s).
- VBOOST: Connect SMU1. Configure it to Voltage Source with a Current Compliance of 200 mA.
- HVOUT / LVOUT: Connect SMU2 to the LDO you want to measure. Configure it to sink current with a Voltage Compliance of 5 V for HVOUT or 2.5 V for LVOUT.

Manipulations

- Impose a voltage between V_{OVCH} and 5 V on SMU1 to force the AEM to start.
- Sweep voltage on SMU1 from V_{OVDIS} + 50 mV to 4.5 V.
- Repeat with different current levels on SMU2 (from 10 µA to 80 mA for HVOUT and from 10 µA to 20 mA for LVOUT). Please make sure to set negative current values on SMU2 to simulate the load.

Measurements

- HVOUT/LVOUT: Measure the voltage.

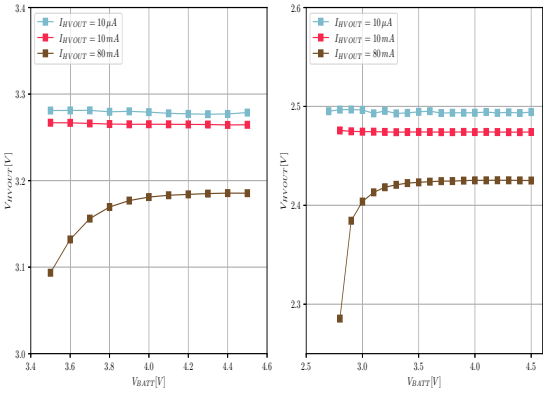


Figure 8: HVOUT at 3.3 V and 2.5 V

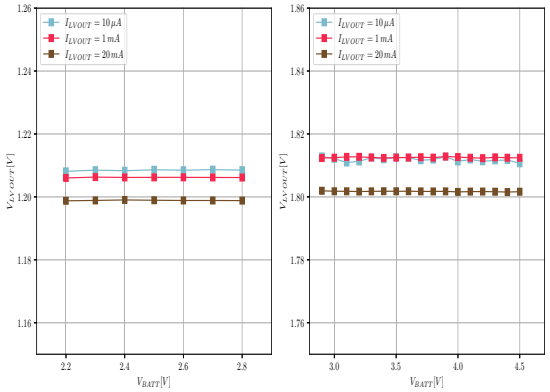


Figure 9: LVOUT at 1.2 V and 1.8 V

4.2. BOOST Efficiency

This test allows users to reproduce the efficiency graphs of the AEM20940 boost converter (Boost Conversion Efficiency Sections of the AEM20940 datasheet).

Setup

- Following steps 1 and 2 explained in the Section 2.1 and referring to Figure 1, configure the board in the desired state.
- VBUCK: Connect a 2.3 V Voltage Source to prevent VBUCK to sink current from VBOOST.
- SRC: Connect SMU1. Configure it to Current Source with a Voltage Compliance of 0 V.
- VBOOST: Connect SMU2 and configure it to Voltage Source with a Current Compliance of 200 mV.
- STATUS[2]: Connect to one of the SMU to detect falling edge.

Manipulations

- Impose a voltage between V_{OVCH} and 5 V on SMU2 to force the AEM to start. When done, impose a voltage between V_{OVDIS} + 50 mV and V_{OVCH}.
- Sweep voltage compliance on SMU1 from V_{OVDIS} + 50 mV to 4.5 V.
- Repeat with different current levels on SMU1 (from 100 µA to 100 mA) and with different voltage levels on SMU2 (from V_{OVDIS} + 50 mV to V_{OVCH}).

Measurements

- STATUS[2]: Dot not make any measurements while high (boost converter is not active during MPP calculation).
- SRC: Measure the current and the voltage.
- VBOOST: Measure the current and the voltage. Repeat the measurement a copious number of times to be sure to capture the current peaks. Figure 10 has been obtained by averaging over 100 measurements configured with a 100 ms integration time.
- Deduce input and output power (P = U x I) and efficiency (η = Pout/Pin).

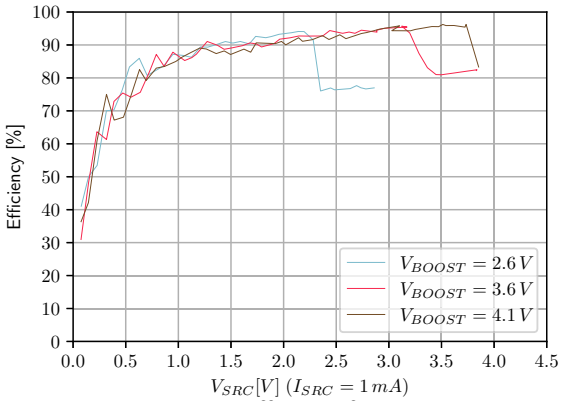
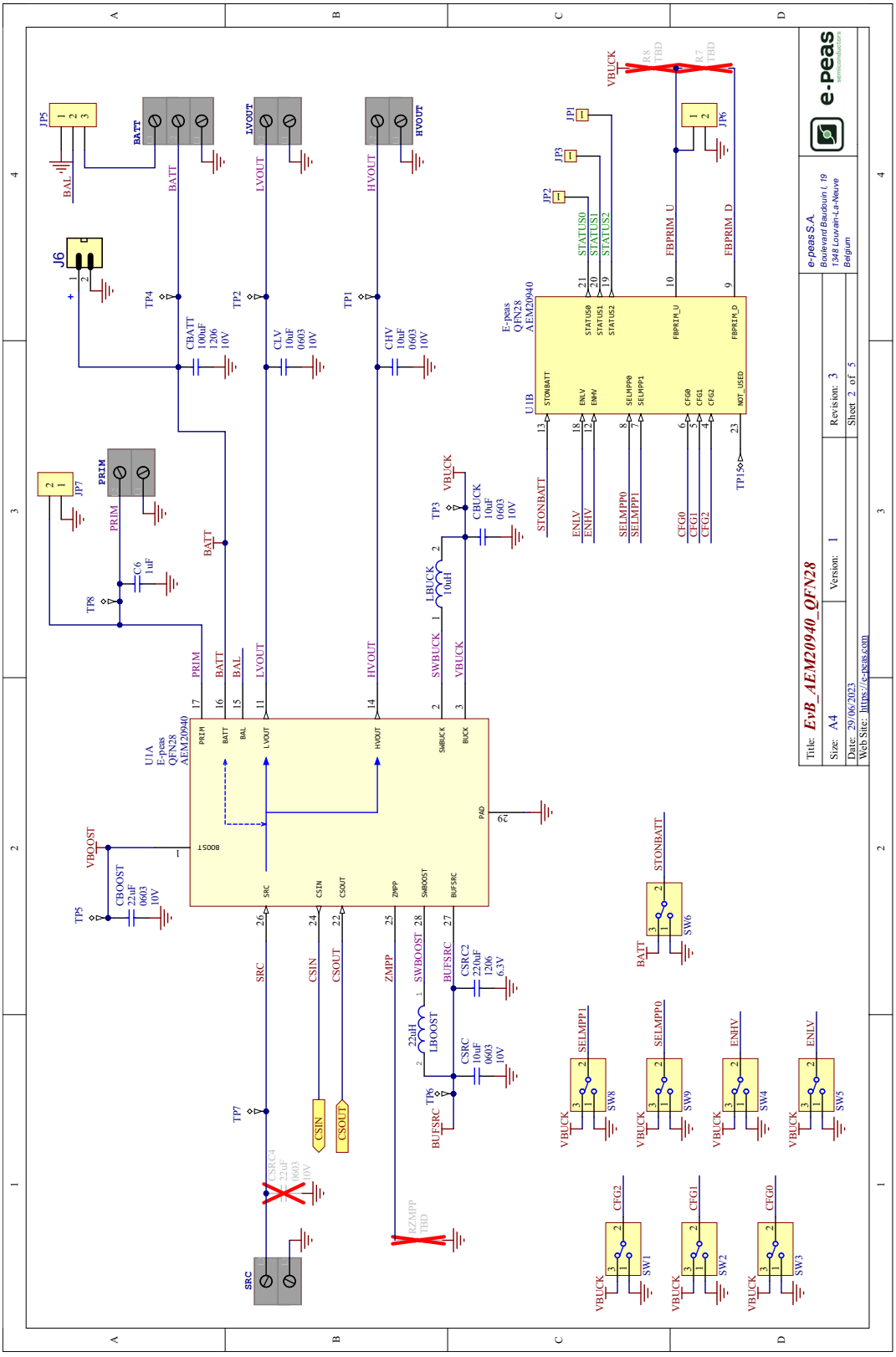


Figure 10: Boost efficiency for ISRC = 1mA

5. Schematic



6. Revision History

EVK Version	User Guide Revision	Date	Description
1.0	1.0	July, 2018	Creation of the document
1.2	1.1	August, 2021	Connection diagram modification
1.3	1.0	August, 2023	Update to EvK version 1.3

Table 5: Revision History