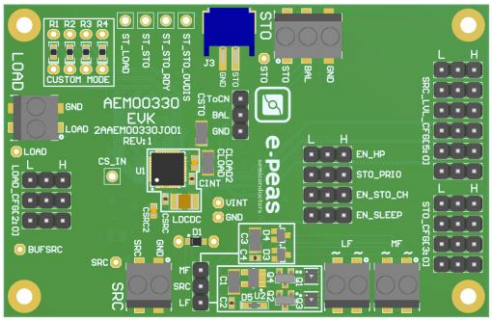
AEM00330
Quick Start Guide EVK



FEATURES

Connectors

- 1 screw connector for the source 2 screw connector for AC input signal
- 1 screw connector 1 JST connector for the Storage Element
- 1 screw connector for the application supply

Configuration

- 6 jumpers SRC_LVL_CFG[x] to define the source voltage regulation
- 4 jumpers STO_CFG[x] to define the storage element protection levels
- 4 resistors footprint related to the custom mode (STO_CFG[3:0]=LHHH)
- 3 jumpers LOAD_CFG[x] to define the LOAD voltage
- 1 jumper to set the dual-cell supercapacitor BAL feature
- 4 jumpers to enable the different modes
- 1 jumper to select the rectifier

Size

- 79mm x 49mm
- 4 x M2.5 Mounting holes

SUPPORT PCB

BOM around the AEM00330

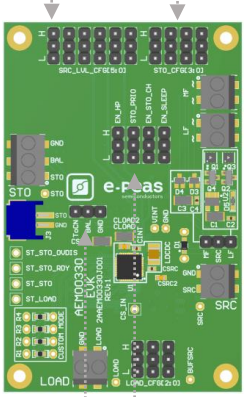
Designator	Description	Quantity	Manufacturer	Link
U1	AEM00330 - Symbol QFN 40-pin	1	e-peas	order at sales@e-peas.com
LDCDC	Power inductor 10 µH - 1.76A	1	Murata	DFE252010F-100M
CLOAD	Ceramic Cap 47 µF, 6.3V, 20%, X5R 0603	1	Murata	GRM188R60J476ME15
CINT	Ceramic Cap 10 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J106ME15
CSRC	Ceramic Cap 15 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J156ME05
CSTO (optional)	Ceramic Cap 100 µF, 6.3V, 20%, X5R 1206	1	TDK	C3216X5R1A107M160AC

Footprint & Symbol: Information available in the datasheet

STEP 1: AEM00330 Configuration

- **Source voltage regulation:** SRC_LVL_CFG[5] – SRC_LVL_CFG[4] – SRC_LVL_CFG[3] – SRC_LVL_CFG[2] – SRC_LVL_CFG[1] – SRC_LVL_CFG[0] (see datasheet for the table)

- **Storage Element voltages protection:** STO_CFG[3] – STO_CFG[2] – STO_CFG[1] – STO_CFG[0]



Configuration pins				Storage element threshold voltages			Typical use
STO_CFG[3]	STO_CFG[2]	STO_CFG[1]	STO_CFG[0]	V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
0	0	0	0	3.00 V	3.50 V	4.05 V	Li-ion battery
0	0	0	1	2.80 V	3.10 V	3.60 V	LiFePO4 battery
0	0	1	0	1.85 V	2.40 V	2.70 V	NiMH battery
0	0	1	1	0.20 V	1.00 V	4.65 V	Dual-cell supercapacitor
0	1	0	0	0.20V	1.00 V	2.60 V	Single-cell supercapacitor
0	1	0	1	1.00 V	1.20 V	2.95 V	Single-cell supercapacitor
0	1	1	0	1.85 V	2.30 V	2.60 V	NGK
0	1	1	1	Custom Mode			
1	0	0	0	1.10 V	1.25 V	1.50 V	Ni-Cd 1 cells
1	0	0	1	2.20 V	2.50 V	3.00 V	Ni-Cd 2 cells
1	0	1	0	1.45 V	2.00 V	4.65 V	Dual-cell supercapacitor
1	0	1	1	1.00 V	1.20 V	2.60 V	Single-cell supercapacitor
1	1	0	0	2.00 V	2.30 V	2.60 V	ITEN / Umal Murata
1	1	0	1	3.00 V	3.50 V	4.35 V	Li-Po battery
1	1	1	0	2.60 V	2.70 V	4.00 V	Tadiran TLI1020A
1	1	1	1	2.60 V	3.50 V	3.90 V	Tadiran HLC1020

- **LOAD voltage:** LOAD_CFG[2] – LOAD_CFG[1] – LOAD_CFG[0]

Configuration pins			LOAD output voltage			
LOAD_CFG[2]	LOAD_CFG[1]	LOAD_CFG[0]	$V_{LOAD,MIN}$	$V_{LOAD,MID}$	$V_{LOAD,TYP}$	$V_{LOAD,MAX}$
0	0	0	3.15 V	3.23 V	3.28 V	3.34 V
0	0	1	2.35 V	2.47 V	2.50 V	2.53 V
0	1	0	1.64 V	1.75 V	1.79 V	1.82 V
0	1	1	1.14 V	1.16 V	1.20 V	1.23 V
1	0	0	1.39 V	1.56 V	1.61 V	2.63 V
1	0	1	1.39 V	1.56 V	1.61 V	4.65 V
1	1	0	Reserved, do not use			
1	1	1				

- **BAL option:** Select “ToCn” for dual-cells supercapacitor and “GND” for any other storage element

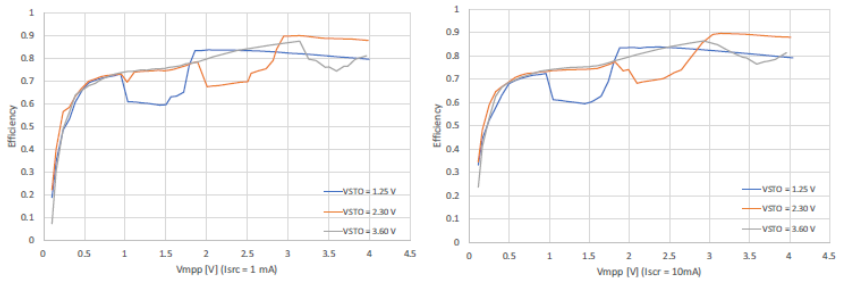
- **Configuration mode:** EN_HP – EN_STO_CH – STO_PRIO – EN_SLEEP
  Connect to H for enabling the feature, connect to L for disabling the feature

STEP 2: Connect the storage element

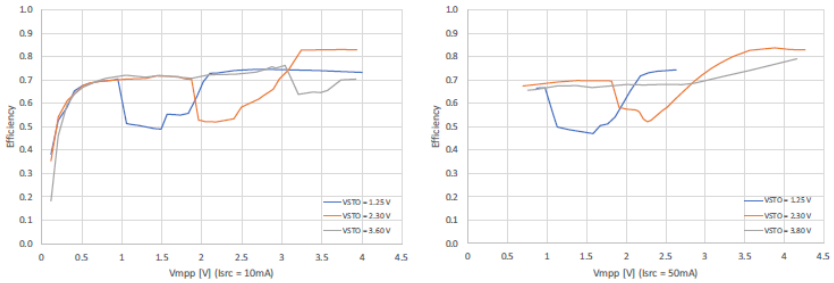
STEP 3: Connect the load to LOAD

STEP 4: Connect the harvester

- **Internal Boost efficiency Vs. input voltage in Low Power mode:**



- **Internal Boost efficiency Vs. input voltage in High Power mode:**



STEP 5: Check the status

Symbol	Logic Level	Low	High
Logic output pins			
ST_STO	Logic output levels on the status STO pin	GND	V_{STO}
ST_LOAD	Logic output levels on the status LOAD pin	GND	V_{LOAD}
ST_STO_RDY	Logic output levels on the status STO_READY pin	GND	V_{LOAD}
ST_STO_OVDIS	Logic output levels on the status BACKUP pin	GND	V_{LOAD}