Ultra-Efficient Smart Power Management IC with Buck Converter Output and 5 V Charger

Features and Benefits

Cold-start capabilities

- Coldstart from the 5 V charger input, or the storage element.

Overdischarge and overcharge protections

- Protection thresholds from 2.30 V to 4.60 V.
- Supports various rechargeable storage element types with preset protection levels or I²C configurations.

Thermal monitoring

- Storage element protections against cold and hot temperatures during charging and discharging.

Regulated output for application circuit

- Output voltage from 2.20 V to 3.30 V.
- Up to 50 mA output current.

System configuration by GPIO or I²C

- Basic configurations through GPIO.
- All setting configurations and system data available through I²C (Fast Mode Plus).

Average Power Monitoring

- Measurement of the power transferred from the storage element to the application circuit.

5 V charger capability

- Charging input for 5 V power supplies.
- Charging current from 50 to 400 mA.
- Optional overvoltage protection up to 20 V.

Shipping mode

- Storage element charge and discharge disabling during shipment.

Product compatibility

- Common pinout and layout-compatible with AEM11920 and AEM11921

Applications

- Remote controls
- Wearables and medical
- PC peripherals
- Smart home and building
- IoT sensors and modules
- Asset trackers

Description

The SPM10140 is an ultra-efficient and compact power management circuit that supplies an application circuit from the energy stored in a storage element through its buck converter with a configurable output voltage.

With its 5 V charger input, the SPM10140 is able to recharge this storage element with a configurable charging current.

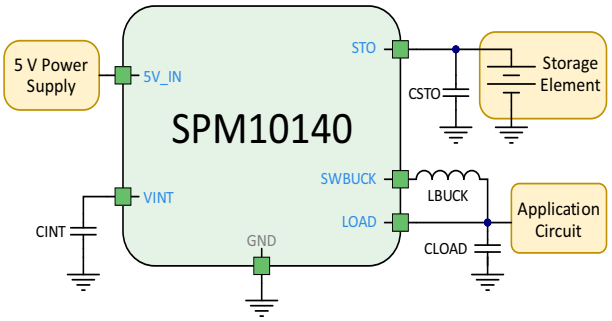
Configurable protection thresholds prevent overcharging and overdischarging the storage element without any additional external components.

I²C communication lets the application MCU control every setting and access SPM10140 data.

The SPM10140's unique Average Power Monitoring (APM) feature allows the application circuit to estimate the energy transferred from the storage element to the application circuit.

Device Information

Description	Part Number
SPM10140, QFN 20-pin, 3 x 3 mm	10SPM10140K0000
SPM10140 - Evaluation board	2ASPM10140K001



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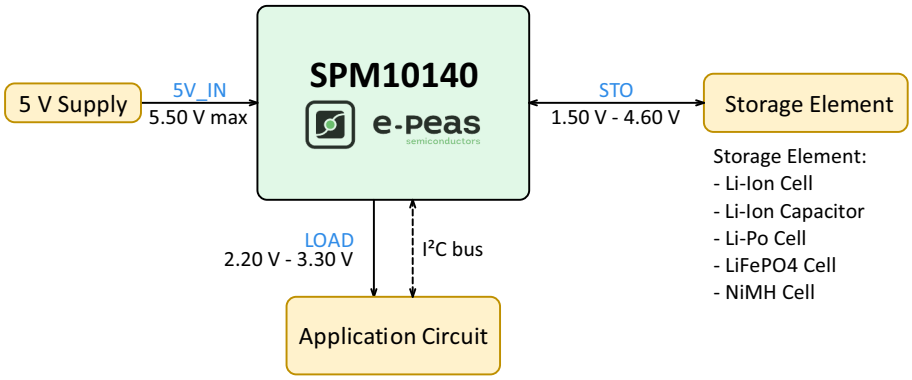


Figure 1: Simplified schematic view

1. Introduction

The SPM10140 is a full-featured energy efficient power management circuit able to supply an application circuit (connected to LOAD) from a storage element (connected to STO) and to charge this storage element from a 5 V power supply. This is done with a minimal bill of material.

The heart of the SPM10140 is composed of a switching buck converter for supplying LOAD with high power conversion efficiency.

The SPM10140 can be configured either by configuration pins for basic configurations or by a set of registers accessed through an I²C bus for advanced configurations.

The 5 V power input 5V_IN allows for charging the storage element using a CC/CV (constant current / constant voltage) method. Additionally, an optional external circuit can be used to protect the SPM10140 from an overvoltage from the external supply connected on 5V_IN.

The SPM10140 can coldstart with a minimum voltage of 1.50 V on the storage element. The cold start is performed either from the 5 V charger input 5V_IN (without the overvoltage protection circuit) or directly from the storage element energy (triggered either by the 5 V supply detection or the SHIP_MODE pin high-to-low transition).

The storage element protection thresholds can be configured between 2 preset configurations through the STO_CFG pin without any additional external component. If those configurations do not fit the user's storage element, the thresholds can be configured individually through I²C registers. The ST_STO status pin provides information about the voltage level of the storage element.

An optional thermal monitoring circuit allows the SPM10140 to protect its storage element by disabling the storage element charge or discharge outside of a configured temperature range.

If the storage element is sufficiently charged, the buck converter provides a regulated output voltage on the LOAD pin, allowing an application circuit to be supplied. The regulated voltage can be set through the LOAD_CFG[1:0] pins or through the I²C registers.

If using I²C, the application circuit connected to the SPM10140 can get an estimate of the energy provided from the storage element to the LOAD output thanks to the Average Power Monitoring (APM) feature.

A shipping mode feature can be enabled through the SHIP_MODE pin, disabling the buck converter, to prevent the discharge of the storage element during shipment.

The SPM10140 features a common pinout with the AEM11920 and AEM11921 that allows for the design of a single PCB layout for an energy harvesting solution (ambient energy harvester and 5 V charger) or a rechargeable solution (5 V charger only).

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2. Pin Configuration and Functions

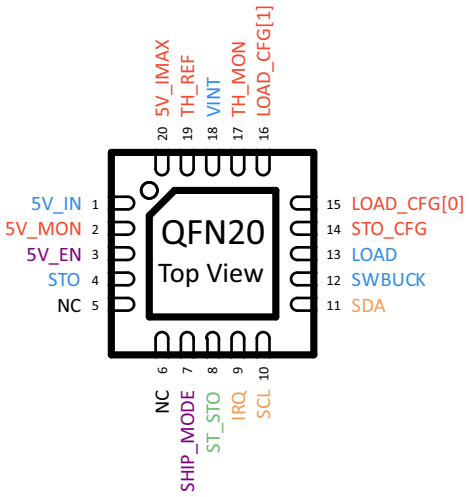


Figure 2: Pinout diagram

Name	Pin	Function
Power pins		
STO	4	Connection to the storage element (rechargeable storage element).
SWBUCK	12	Switching node of the buck converter. If not used: - Disable buck converter through LOAD_CFG[1:0] pins or BUCKCFG.EN register field. - Leave the SWBUCK pin floating.
LOAD	13	Output voltage of the buck converter to supply an application circuit. If the LOAD output is not used: - Disable buck converter through LOAD_CFG[1:0] pins or BUCKCFG.EN register field. - If the I²C interface is used, connect the LOAD pin to STO or to any external voltage less than or equal to V_{STO}. - If the I²C interface is not used, leave the LOAD pin floating.
5V_IN	1	Input of the 5 V DC power supply. Leave floating if not used.
VINT	18	Connection for C_{INT} buffering capacitor. SPM10140 internal power supply (do not connect any external circuit on VINT).

Table 1: Pins description (part 1)

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Name	Pin	Logic level		Function
		LOW	HIGH	
Configuration pins				
STO_CFG	14	GND	VINT	Used to configure the storage element protection thresholds (see Section 6.2). Read as HIGH if left floating.
LOAD_CFG[1]	16	GND	VINT	Used to configure the LOAD output regulation voltage (see Section 6.3). Read as HIGH if left floating.
LOAD_CFG[0]	15	GND	VINT	
TH_REF	19	Analog Pin		Reference voltage for thermal monitoring (see Section 5.4). Leave floating if not used.
TH_MON	17	Analog Pin		Connection for the mid-point of the thermal monitoring voltage divider (see Section 5.4). Connect to VINT if not used.
5V_MON	2	Analog Pin		5 V DC power supply monitoring pin. Connect to GND if the overvoltage protection circuit is not used.
5V_IMAX	20	Analog Pin		Connection to an external resistor to set the charging current from the 5V_IN supply to STO (see Section 5.6). Leave floating if the 5 V charger is not used.
Control pins				
5V_EN	3	GND	STO	Output pin used to enable the power path between the 5 V DC supply and the SPM10140 5V_IN pin when the overvoltage protection circuit is used (see Section 5.6.2). Leave floating if the overvoltage protection circuit is not used.
SHIP_MODE	7	GND	STO	Used to configure the shipping mode. When HIGH: - Minimum consumption from the storage element. - Buck (LOAD) is disabled. Cannot be left floating, connect to GND if not used.
I²C pins				
SCL	10	GND	LOAD	Unidirectional serial clock for I²C communication. Connect a pull-up resistor to LOAD if used (see Section 6.1.2). Connect to GND if not used.
SDA	11	GND	LOAD	Bidirectional data line for I²C communication. Connect a pull-up resistor to LOAD if used (see Section 6.1.2). Connect to GND if not used.
IRQ	9	GND	LOAD	Logic output signal to indicate SPM10140 events to an external circuit GPIO. Leave floating if not used.
Status pin				
ST_STO	8	GND	STO	Logic output. - HIGH when in SUPPLY STATE (see Section 5.9). - LOW otherwise. Leave floating if not used.
Other pins				
GND	Exposed pad			Ground connection, must be strongly tied to the PCB ground plane.
NC	5, 6			Not connected pins, leave floating.

Table 2: Pins description (part 2)

NOTE: The SPM10140 shares a common pinout and footprint with the AEM11920 and AEM11921 with the exception of pins 5, 6, and 20, that are used in a version and NC for the other version (see pins description tables). To design a single PCB layout for both AEM1192x and SPM10140, ensure pins 5, 6, and 20 are routed appropriately to match both parts.

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3. Specifications

3.1. Absolute Maximum Ratings

Parameter		Min	Max	Unit
Operating junction temperature T_J		-40	125	°C
Storage temperature T_{stg}		-55	150	°C
Input voltage	STO, SWBUCK, 5V_IN, 5V_MON, 5V_IMAX, LOAD, 5V_EN, SHIP_MODE, SCL, SDA, IRQ, ST_STO.	-0.30	5.50	V
	VINT, STO_CFG, LOAD_CFG[1:0], TH_REF, TH_MON.	-0.30	2.75	V

Table 3: Absolute maximum ratings

CAUTION: The voltage on LOAD pin must always remain lower or equal than the voltage on the STO pin.

3.2. ESD Ratings

Parameter		Value	Unit
Electrostatic discharge V_{ESD}	Human-Body Model (HBM)[1]	± 2000	V
	Charged-Device Model (CDM)[2]	± 1000	V

Table 4: ESD ratings

1. ESD Human-Body Model (HBM) value tested according to JEDEC standard JS-001-2024.
2. ESD Charged-Device Model (CDM) value tested according to JEDEC standard JS-002-2025.

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

3.3. Thermal Resistance

Package	Parameter	Value	Unit
QFN 20-pin 3 x 3 mm	Junction-to-Ambient (θJA)	50[1]	°C/W
	Junction-to-Case (θJC)	7	°C/W

Table 5: Thermal data

1. Typical value for the SPM10140 in QFN 20-pin 3 x 3 mm. The effective junction-to-ambient thermal resistance heavily depends on PCB design and application environment. Refer to Section 13.3 for detailed information.

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3.4. Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power conversion						
V_{5V_IN}	Voltage on the 5V_IN pin to allow for charging the storage element.		max (3.70, V_{STO} + 0.25)[1]		5.50	V
$V_{5V_MON,OVP}$	5V_MON pin voltage above which the 5 V charger overvoltage protection (OVP) circuit is triggered.			1.00		V
$I_{5V,CC}$	Maximum charging current of the 5 V charger (5V_IN input), configurable through 5V_IMAX.	In constant current (CC) mode when $V_{STO} \geq V_{OVDIS}$	50		400	mA
$I_{5V,OVDIS,CC}$	Charging current of the 5 V charger (5V_IN input) in overdischarge.	In constant current (CC) mode when $V_{STO} < V_{OVDIS}$		36		mA
$I_{5V,CV,MIN}$	Termination current of the 5 V charger (5V_IN input) in constant voltage (CV) mode.			0.1 x $I_{5V,CC}$		mA
V_{LOAD}	Voltage on LOAD.	Buck converter output (LOAD) enabled.	2.20		3.30	V
		Buck converter output (LOAD) disabled.	1.50		V_{STO}[2]	V
$I_{LOAD,MAX}$	Maximum current from the LOAD pin.	L_{BUCK} = 10 µH		50		mA

Table 6: Electrical characteristics (part 1)

1. The 5 V charger is considered connected when the voltage on 5V_IN is greater than or equal to 3.70 V and at least 250 mV higher than the voltage on STO. It can be actively charging or not.
2. If the buck converter is disabled, the LOAD pin can be supplied by shorting LOAD to STO or to any external voltage less than or equal to V_{STO} to use the I²C interface. The voltage on the LOAD pin must always remain lower or equal to the voltage on the STO pin.

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timings						
$T_{CRIT,ST}$	Delay triggered when V_{STO} drops below V_{OVDIS}. The SPM10140 sets ST_STO LOW if V_{STO} remains below V_{OVDIS} once $T_{CRIT,ST}$ elapses (see Section 5.9).			1.63		s
$T_{CRIT,OVDIS}$	Delay triggered when V_{STO} drops below V_{OVDIS}. The SPM10140 switches to OVDIS STATE once $T_{CRIT,OVDIS}$ elapses (see Section 5.9).			2.27		s
$T_{CRIT,LOAD}$	Delay triggered when V_{STO} drops below $V_{OVDIS,BUCK}$ or when the temperature goes outside the discharge temperature range. The SPM10140 sets IRQFLG0.LOADSHTDWN register field HIGH if V_{STO} remains below $V_{OVDIS,BUCK}$ or if the temperature remains outside of the range once $T_{CRIT,LOAD}$ elapses (see Section 5.2).			1.63		s
$T_{LOAD,DIS}$	Delay triggered when V_{STO} drops below $V_{OVDIS,BUCK}$ or when the temperature goes outside the discharge temperature range. The SPM10140 disables its LOAD output once $T_{LOAD,DIS}$ elapses (see Section 5.2).			2.27		s
$T_{GPIO,MON}$	GPIO monitoring rate.			1.86		s
$T_{STO,MON}$	Storage element voltage monitoring rate.	When the buck converter is disabled and the 5 V charger is not charging.		116		ms
		When the buck converter is enabled or the 5 V charger is charging.		15		ms
$T_{5V,MON}$	External 5 V charger voltage monitoring rate when the charger is not charging (see Section 5.6.2).			0.47		s
$T_{TEMP,MON}$	Temperature monitoring rate.			7.45		s
$T_{APM,WINDOW}$	Average Power Monitoring (APM) time window (see Section 5.5).			0.93		s
$T_{PRE,TMR}$	5 V charger pre-charge timer duration (see Section 5.6.3).	GPIO configuration	30		120	min
		I²C configuration	15		120	min
$T_{CC/CV,TMR}$	5 V charger CC/CV timer duration (see Section 5.6.3).	GPIO configuration		10		h
		I²C configuration	2.5		20	h
$T_{SHIP,IGNORE}$	Delay during which the SPM10140 ignores the SHIP_MODE pin state (see Section 5.8).			7.45		s

Table 7: Electrical characteristics (part 2)

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Storage element						
V_{STO}	Voltage on the storage element.		1.50		4.60	V
V_{OVDIS}	Voltage below which the storage element is considered to be fully depleted, and must not be discharged any further (see Section 5.3).	Configured by STO_CFG.	2.50		3.00	V
		Configured by I²C.[1]	2.30		3.50	V
V_{CHRDY}	In START STATE, voltage required on the storage element to switch to SUPPLY STATE when the 5 V charger is not charging (see Section 5.3).	Configured by STO_CFG.	2.60		3.20	V
		Configured by I²C.[1]	2.40		3.60	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging (see Section 5.3).	Configured by STO_CFG.	3.80		4.15	V
		Configured by I²C.[1]	2.70		4.60	V
$V_{OVDIS,BUCK}$	Minimum voltage accepted on the storage element before: - Starting to supply the LOAD if the 5 V charger is charging, - Stopping to supply the LOAD when the storage element voltage is too low. (See Section 5.3).			max(V_{OVDIS}, V_{LOAD})		V
$V_{CHRDY,BUCK}$	Minimum voltage accepted on the storage element before starting to supply the LOAD if the 5 V charger is not charging (see Section 5.3).	Configured by STO_CFG depending on V_{LOAD}.	2.60		3.50	V
		Configured by I²C.[2]	max (2.40, V_{LOAD})		3.60	V
V_{HYST}	Storage element overcharge hysteresis voltage (see Section 5.3).	Configured by STO_CFG.	0		37.5	mV
		Configured by I²C.	0		112.5	mV
$V_{OVCH,LOW}$	Voltage on STO below which the SPM10140 resumes charging the storage element (see Section 5.3).			V_{OVCH} - V_{HYST}		V

Table 8: Electrical characteristics (part 3)

1. Ensure that $V_{OVDIS} < V_{CHRDY} < V_{OVCH}$ with sufficient margin to prevent unintended state changes due to small voltage variation on the storage element.

2. If $V_{CHRDY,BUCK}$ is configured by I²C below $V_{OVDIS,BUCK}$, it will be automatically set equal to $V_{OVDIS,BUCK}$. Nevertheless, a minimum margin of 100 mV must always be maintained between $V_{OVDIS,BUCK}$ and $V_{CHRDY,BUCK}$ to prevent toggling of the buck converter enable state. Furthermore, $V_{CHRDY,BUCK}$ must never be configured below V_{LOAD}.

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC characteristics						
$V_{ADC,STEP}$	Voltage step size for one ADC step of the temperature monitoring (see Section 6.5.2).			3.90		mV
Internal supply & quiescent current						
V_{INT}	Internal voltage supply.			2.25		V
$V_{INT,RESET}$	Minimum voltage on VINT before switching to RESET STATE (from any other state).			2.00		V
$V_{INT,CS}$	Minimum voltage on VINT to allow the SPM10140 to switch from RESET STATE to SENSE STO STATE.			2.30		V
$I_{Q,SUPPLY}$	SPM10140 internal quiescent current on STO in SUPPLY STATE.	Buck enabled (LOAD)[1].		590		nA
		Buck disabled (LOAD).		265		nA
$I_{Q,SHIP}$	SPM10140 internal quiescent current on STO in shipping mode (SHIP_MODE set HIGH).			12	150	nA
$I_{Q,RESET}$	SPM10140 internal quiescent current on STO in RESET STATE.			12	50	nA

Table 9: Electrical characteristics (part 4)

1. The LOAD pin is left floating.

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3.5. Recommended Operating Conditions

Symbol	Parameter		Min[1]	Typ	Max[1]	Unit
External components						
L_{BUCK}	Buck converter inductor (optional[2]).		10	10		µH
C_{LOAD}	Buck converter decoupling capacitor (optional[2]).		10	22		µF
C_{INT}	VINT terminal decoupling capacitor (mandatory).		5	10		µF
C_{STO}	STO terminal decoupling capacitor (mandatory).		5	47		µF
R_{5V_IMAX}	5 V charger maximum current configuration resistor (optional[3]).		150		1200	Ω
C_{5VIN}	5V_IN terminal decoupling capacitor (optional[3]).		22	47		µF
R_{5VIN}	5 V charger RC filter resistor (optional[3]).			1		Ω
Q_1	5 V charger overvoltage protection (OVP) circuit PMOS (optional[4]).	$V_{GS(TH)}$			3.25	V
		$R_{DS(ON)}$			200	mΩ
		C_{iss}			1	nF
Q_2	5 V charger OVP circuit NMOS (optional[4]).	$V_{GS(TH)}$			1.50	V
		C_{iss}			200	pF
R_{5VPU}	5 V charger OVP circuit pull-up resistor (optional[4]).			1		kΩ
R_{5VDIV1}	5 V charger OVP circuit voltage divider resistor 1 (optional[4]).			44.2		kΩ
R_{5VDIV2}	5 V charger OVP circuit voltage divider resistor 2 (optional[4]).			10		kΩ
R_{SDA} / R_{SCL}	I²C interface pull-up resistors (optional[5]).			1		kΩ
R_{TH}	NTC thermistor used for thermal monitoring operation (optional[6]).	R0		10^{7}	250	kΩ
		Beta		3380^{7}		K
R_{DIV}	Resistor used to create a voltage divider with R_{TH} for thermal monitoring operation (optional[6]).		4	22^{7}	40	kΩ
Operating temperatures						
T_A	Operating ambient temperature.		-40		85^{8}	°C
T_J	Operating junction temperature.		-40		110	°C

Table 10: Recommended operating conditions

1. All minimum and maximum values are effective components values, taking into account tolerances, derating, temperatures, voltages and any operating conditions (special care must be taken with capacitor derating).
2. Required only if buck converter is used.
3. Required only if the 5 V charger is used, using C_{5VIN} and R_{5VIN} is recommended when not using the optional 5 V charger OVP circuit but mandatory when using the OVP circuit.
4. Required only is the 5 V charger OVP circuit is used.
5. Required only if the I²C interface is used. For more information on how to select the value of these resistors, refer to "Pull-up resistor sizing" section in NXP's UM10204 "I²C-bus specification and user manual".
6. Required only if the temperature monitoring feature is used.
7. Those values allow for having the default temperature thresholds at startup shown in Table 14.
8. Maximum operating ambient temperature with the typical junction-to-ambient thermal resistance (Table 5), a 5 V charger maximum current equal to 180 mA and V_{OVDIS} equal to 2.30 V. For other operating conditions, refer to Section 13.3 to estimate the effective maximum TA.

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3.5.1. External Inductors Information

The SPM10140 operates with one external miniature inductor. It must support a minimum switching frequency of 10 MHz. Using an inductor with low equivalent series resistance (ESR) improves the power-conversion efficiency of the buck converter.

L_{BUCK}

With the recommended operating conditions (10 µH inductor), the buck inductor L_{BUCK} must support a minimum peak current of 135 mA.

3.5.2. External Capacitors Information

The SPM10140 operates with three external miniature capacitors to ensure stable operation of the buck converter output, storage element output, and internal supply. Each capacitor serves as a local energy buffer that limits voltage fluctuations caused by switching activity or dynamic load transition.

To maintain optimal performances and minimized quiescent current, all capacitors must exhibit a low leakage current and follow the recommended nominal values listed in Table 10, with a tolerance of ± 20 %.

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3.6. Typical Characteristics

3.6.1. Buck Converter Conversion Efficiency

Figure 3 shows the SPM10140 buck efficiency with L_{BUCK} = 10 µH (TDK VLS252012CX-100M-1).

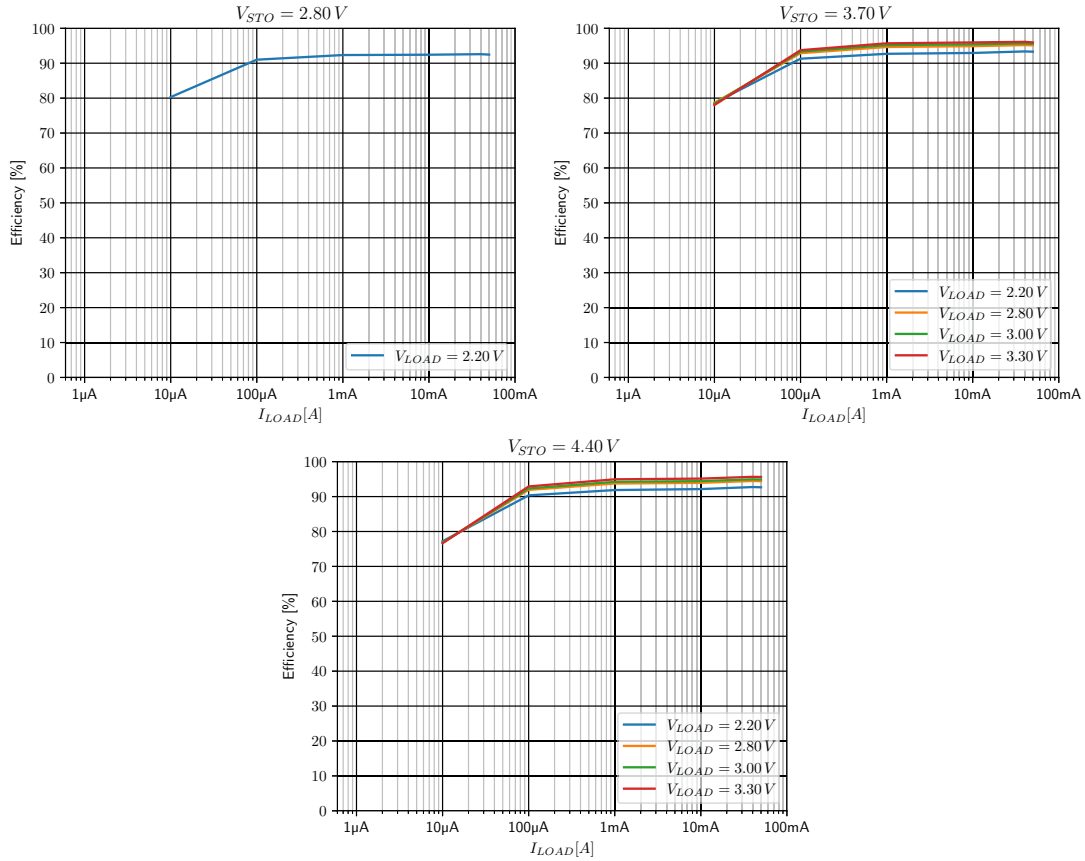


Figure 3: STO to LOAD efficiency vs I_{LOAD}

NOTE: The buck efficiency graphs have been measured with the external components recommended in Section 12.

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4. Functional Block Diagram

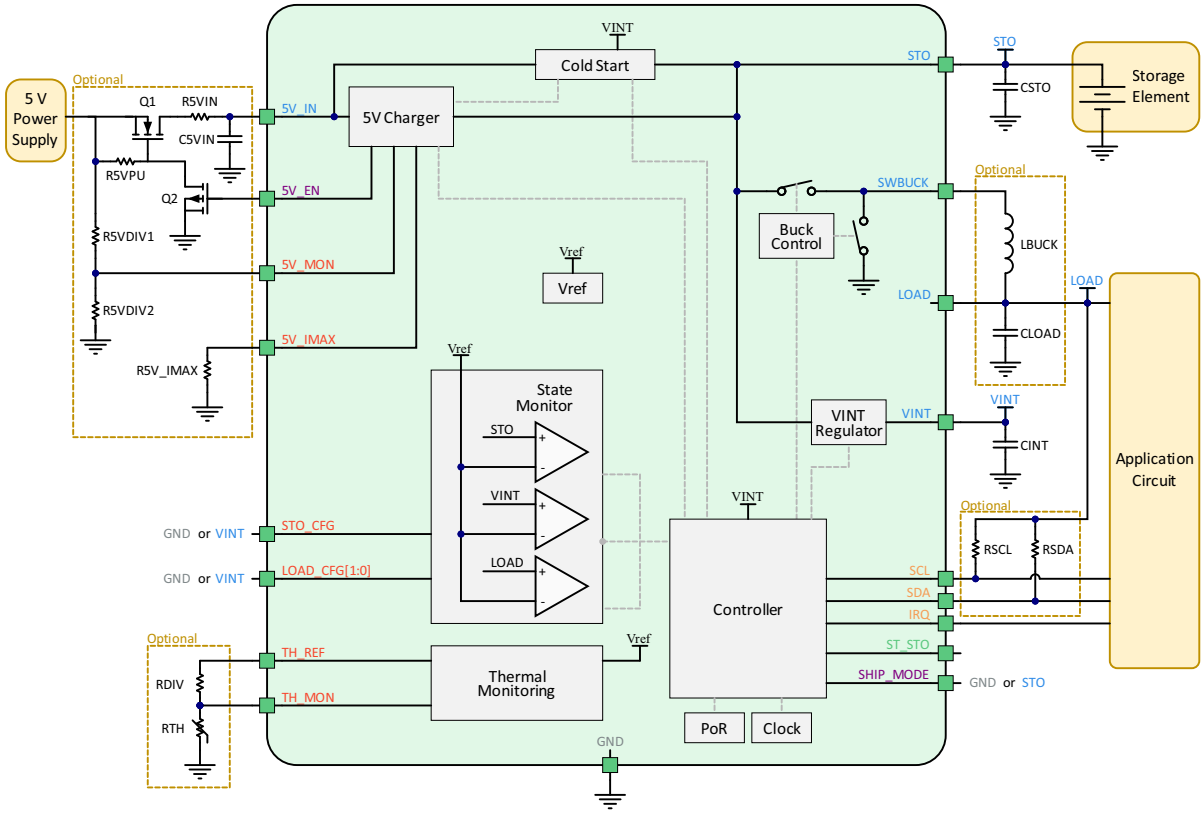


Figure 4: Functional block diagram

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5. Theory of Operation

5.1. Cold-Start Circuits

The SPM10140 is able to coldstart from the 5 V power supply input 5V_IN (without overvoltage protection circuit) or directly from the storage element energy (triggered either by the 5 V supply detection or the SHIP_MODE pin high-to-low transition). The cold-start circuit provides energy to the SPM10140 internal supply (VINT) when the device is in RESET STATE, SENSE STO STATE or OVDIS STATE.

5.2. Buck Converter

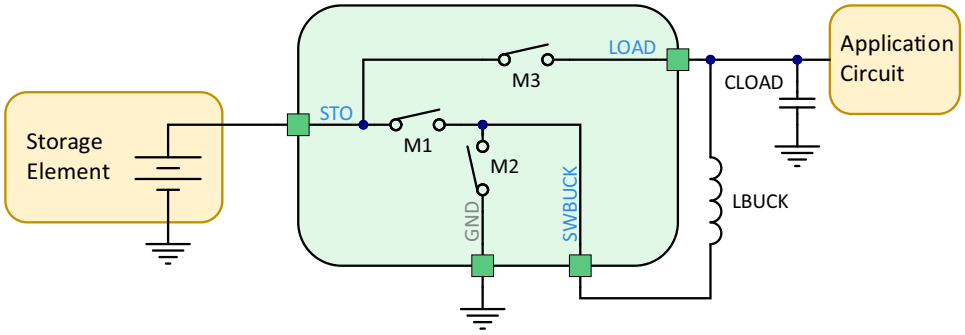


Figure 5: Simplified schematic view of the buck converter

The buck (step-down) converter transfers energy from the storage element connected to STO to the regulated LOAD output. The switching transistors of the buck converter are M1 and M2. The reactive power component of this converter is the external inductor L_{BUCK}. LOAD is decoupled by the capacitor C_{LOAD}, which smooths the voltage against the current pulses from the buck converter and the consumption of the external circuit connected to LOAD.

Setting the LOAD regulation voltage V_{LOAD} or disabling the buck converter is done through the LOAD_CFG[1:0] pins (see Section 6.3) or the I²C register BUCKCFG (see Section 9.3).

Using the buck converter is not mandatory. If not used, the user must do the following:

- Connect all LOAD_CFG[1:0] to GND (LOW) to disable the buck converter.
- Leave SWBUCK floating.
- If not using the I²C interface, leave LOAD floating.
- If using the I²C interface, short the LOAD pin to STO, or to any external supply with a voltage less than or equal to V_{STO}, to continue supplying the I²C bus even if the buck converter is disabled.

5.2.1. Normal Mode

After cold start, if the buck converter is enabled and if the temperature is within the discharge temperature range, the buck converter starts:

- When V_{STO} is higher than $V_{CHRDY,BUCK}$ if the 5 V charger is not charging the storage element.
- When V_{STO} is higher than $V_{OVDIS,BUCK}$ if the 5 V charger is charging the storage element or if exiting the shipping mode.

When V_{STO} drops below $V_{OVDIS,BUCK}$, the SPM10140 waits for $T_{CRIT,LOAD}$ to set IRQFLG0.LOADSHTDWN register field HIGH and to schedule to disable the buck converter. The LOAD output remains enabled until the end of $T_{LOAD,DIS}$.

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When the temperature gets out of the storage element discharge temperature range (TEMPCOLDDIS and TEMPHOTDIS), the SPM10140 rises the IRQFLG0.TEMPDIS and waits for $T_{CRIT,LOAD}$. If the temperature is still out of range after $T_{CRIT,LOAD}$, the SPM10140 schedules to disable the buck converter. The LOAD output remains enabled until the end of $T_{LOAD,DIS}$.

When the difference between V_{STO} and V_{LOAD} is too small for the buck converter to keep working properly, it switches to "bang-bang" controlled converter mode:

- When V_{LOAD} is too low, the switch M3 connects STO directly to LOAD, making V_{LOAD} rise.
- When V_{LOAD} is too high, M3 disconnects STO and LOAD so that V_{LOAD} decreases.

This happens when the following condition is satisfied:

$$V_{STO} - V_{LOAD} < 0.25\ V$$

In that case, efficiency is lower than in buck mode.

5.2.2. Bypass Mode

To maintain the buck converter output (LOAD) enabled when V_{STO} drops below $V_{OVDIS,BUCK}$, the buck converter bypass mode can be used. In this mode, the buck converter behavior is the same as in the normal mode except when the storage element voltage drops below $V_{OVDIS,BUCK}$ for more than $T_{CRIT,LOAD}$.

At this moment, instead of disabling the buck converter output after $T_{LOAD,DIS}$, the LOAD pin is internally shorted to the STO pin. The SPM10140 continues to supply the LOAD output with $V_{LOAD} = V_{STO}$ until one of the following:

- The storage element voltage recovers above $V_{CHRDY,BUCK}$. In this case, the SPM10140 buck convert switches back to normal mode.
- The storage element voltage drops below V_{OVDIS}. In this case, the SPM10140 waits for $T_{CRIT,LOAD}$ to set IRQFLG0.LOADSHTDWN register field HIGH and to schedule to disable the buck converter. The LOAD output remains enabled until the end of $T_{LOAD,DIS}$.

The buck converter bypass mode is disabled by default. It can be enabled through the BUCKCFG.BYPASSEN I²C register field (see Section 9.3).

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5.3. Storage Element Protections

To support various storage element types, prevent storage element degradation and ensure physical safety, the SPM10140 allows the configuration of several protection thresholds.

The storage element voltage thresholds allow to protect the storage element against over charging or discharging:

- Overdischarge threshold (V_{OVDIS}): required voltage to switch from START STATE to SUPPLY STATE when the 5 V charger is charging or if the shipping mode is exited. V_{OVDIS} threshold is also the voltage below which the storage element is considered to be fully depleted, and must not be discharged any further.
- Overdischarge buck threshold ($V_{OVDIS,BUCK}$): required voltage on the storage element to enable the buck converter output (LOAD) if the 5 V charger is charging or if the shipping mode is exited. $V_{OVDIS,BUCK}$ threshold is also the voltage below which the buck converter output (LOAD) is disabled to stop discharging the storage element.
- Charge-ready threshold (V_{CHRDY}): required voltage on the storage element to switch from START STATE to SUPPLY STATE when the 5 V charger is not charging and if the SPM10140 has not just exited shipping mode.
- Charge-ready buck threshold ($V_{CHRDY,BUCK}$): required voltage on the storage element to enable the buck converter output (LOAD) if the 5 V charger is not charging and if the SPM10140 has not just exited shipping mode.
- Overcharge threshold (V_{OVCH}): maximum voltage accepted on the storage element before disabling its charging.
- Overcharge low threshold ($V_{OVCH,LOW}$): Once the V_{OVCH} threshold is detected, the SPM10140 wait for the storage element to drop to $V_{OVCH,LOW}$ before resuming the storage element charge. $V_{OVCH,LOW}$ can be modified by configuring V_{HYST}:

$$V_{OVCH,LOW} = V_{OVCH} - V_{HYST}$$

The storage element temperature thresholds allow to protect the storage element in hot and cold environments thanks to the thermal monitoring feature (see Section 5.4):

- Minimum charging temperature (TEMPCOLDCH): temperature below which the storage element charge is disabled.
- Maximum charging temperature (TEMPHOTCH): temperature above which the storage element charge is disabled.
- Minimum discharging temperature (TEMPCOLDDIS): temperature below which the buck converter output (LOAD) is disabled to stop discharging the storage element.
- Maximum discharging temperature (TEMPHOTDIS): temperature above which the buck converter output (LOAD) is disabled to stop discharging the storage element.
- Temperature monitoring hysteresis (TEMPPROTECT.HYST): configurable hysteresis for the thermal protection thresholds.

See Section 6.2 for further information about the storage element thresholds configuration.

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5.4. Thermal Monitoring

The SPM10140 thermal monitoring allows for monitoring the ambient temperature and comparing it with the configured charge and discharge protection thresholds to protect the storage element from cold and hot temperatures.

To use the thermal monitoring feature, a resistor (R_{DIV}) and a NTC thermistor (R_{TH}) are required in order to form a voltage divider (see Section 6.5). The TH_REF pin allows for applying a reference voltage to the voltage divider while TH_MON is the measuring point. The temperature evaluation is done periodically every $T_{TEMP,MON}$ (see Table 7). To spare power, the divider is biased only during this evaluation.

Based on the temperature monitoring, the SPM10140 is able to protect the storage element with the configured temperature thresholds (see Section 5.3 and Section 6.5).

The thermal monitoring is optional. If not used, connect TH_MON to VINT and leave TH_REF floating.

5.5. Average Power Monitoring

The SPM10140 Average Power Monitoring (APM) feature is used to measure the energy transferred from the storage element to the buck converter output LOAD (APMLOAD).

Please note that the APM measure is related to STO (energy provided from the storage) as shown on Figure 6.



Figure 6: Average Power Monitoring in the power chain

The APM module is able to determine the transferred energy by counting the number of current pulses transferred from STO to LOAD by the buck converter over a fixed time window $T_{APM,WINDOW}$ (see Table 7), and thus, evaluates the corresponding energy.

Refer to Section 9.12 for further details about how to convert registers value to Joules.

5.5.1. APM IRQ

If the IRQEN1.APMDONE field has been set to 1 (see Section 9.9.2), a rising edge on the IRQ pin along with the IRQFLG1.APMDONE field indicates the end of an APM window and thus, that new APM values are available and ready to be read in the APM data register (see Section 9.12).

When the IRQ pin rises due to the IRQFLG1.APMDONE,the APM data registers should be read before the end of the next APM window, after which the APM data will be overwritten.

5.6. 5 V Charger

The SPM10140 is equipped with a 5 V charger (5V_IN) that can be used for charging the storage element (STO) when the following conditions are met:

- $V_{5V_IN} \geq 3.70$ V.
- $V_{5V_IN} \geq V_{STO} + 250$ mV.
- The temperature is within the configured operating range for charging.
- The SPM10140 is either in START STATE, SUPPLY STATE, or OVDIS STATE.

The 5 V charger operates in CC/CV mode (see Section 5.6.1) and can be protected with an optional overvoltage external protection circuit (see Section 5.6.2). Two watchdog timers can be configured for the 5 V charger (see Section 5.6.3).

Using the 5 V charger is not mandatory. When not used, leave 5V_IN pin floating.

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5.6.1. CC/CV Mode

The SPM10140 5 V charger uses a CC/CV method to charge the storage element. As represented in Figure 7, the charging current depends on the storage element voltage:

- (1) Constant current (CC) mode in overdischarge: the SPM10140 charges the storage element with a constant current equal to $I_{5V,OVDIS,CC}$ as long as V_{STO} is below V_{OVDIS}.
- (2) Constant current (CC) mode: the SPM10140 charges the storage element with a constant current equal to the configured $I_{5V,CC}$ when V_{STO} is neither overdischarged nor overcharged. $I_{5V,CC}$ is configured by R_{5V_IMAX} resistor connected between 5V_IMAX pin and GND (see Section 6.4.1 for further details about R_{5V_IMAX} configuration).
- (3) Constant voltage (CV) mode: the SPM10140 maintains the storage element voltage to V_{OVCH} by gradually reducing the charging current until it drops to $I_{5V,CV,MIN}$.
- (4) End of charge: the SPM10140 stops charging the storage element as the charging current reached the termination current $I_{5V,CV,MIN}$. The storage element charge is resumed when V_{STO} drops below $V_{OVCH,LOW}$.

See Table 6 for $I_{5V,OVDIS,CC}$, $I_{5V,CC}$, and $I_{5V,CV,MIN}$ values.

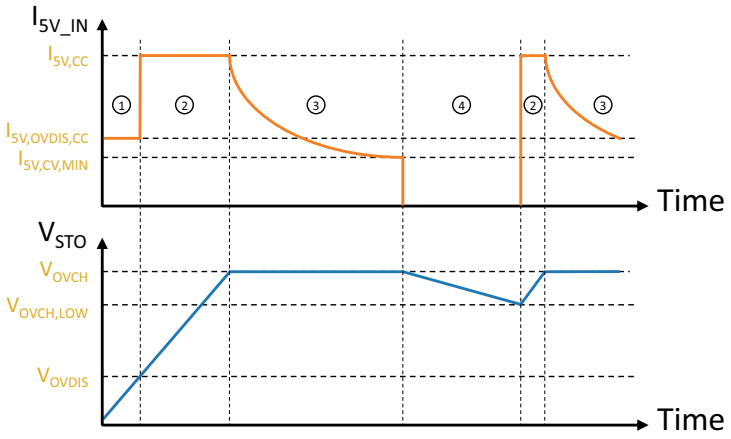


Figure 7: Charging phases of the 5 V charger

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5.6.2. Overvoltage Protection (OVP) Circuit

To protect the SPM10140 from voltages higher than 5.50 V on the 5V_IN pin, an external overvoltage protection (OVP) circuit can be used.

To use this protection circuit, some additional components are required (see Figure 8):

- R_{5VIN} and C_{5VIN} are used as a RC filter.
- R_{5VDIV1} and R_{5VDIV2} are used as a voltage divider to monitor the 5 V external supply voltage.
- Q_1, Q_2, and R_{5VPU} are used to enable or disable the path between the 5 V external supply and the SPM10140 5V_IN pin.

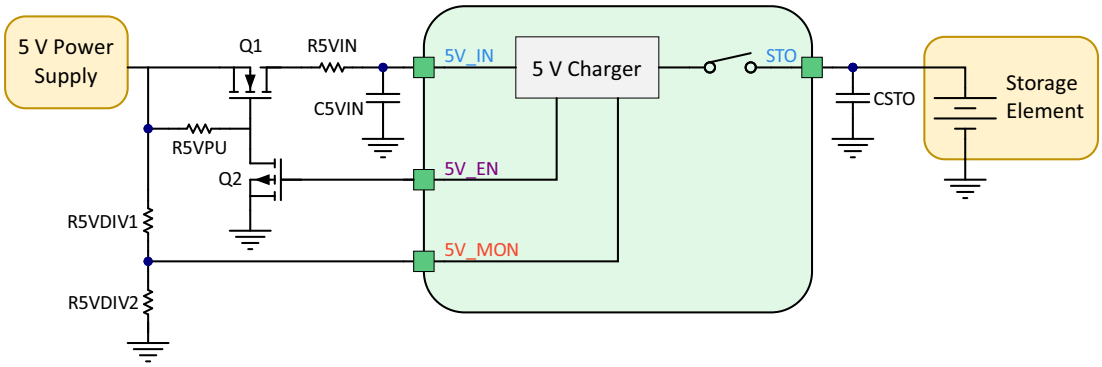


Figure 8: 5 V charger overvoltage (OVP) external circuit

When using the 5 V charger OVP circuit, the SPM10140 monitors the external 5 V supply voltage through a voltage divider every $T_{5V,MON}$. When V_{5V_MON} is measured below $V_{5V_MON,OVP}$ (see Table 6), the SPM10140 sets 5V_EN pin HIGH to enable the path between the 5 V power supply and the SPM10140 5V_IN pin. From this point, the 5 V supply voltage is monitored continuously through 5V_MON pin. If V_{5V_MON} rises above $V_{5V_MON,OVP}$, the SPM10140 instantly sets 5V_EN pin LOW to stop charging through the 5 V charger and protect itself from overvoltage on 5V_IN.

The overvoltage protection circuit disconnects the 5V_IN pin from the 5 V power supply when the following condition is true:

$$\text{5 V power supply voltage} > V_{5V_MON,OVP} \times \frac{R_{5VDIV1} + R_{5VDIV2}}{R_{5VDIV2}}$$

With the recommended R_{5VDIV1} and R_{5VDIV2} values (see Table 10), this mechanism triggers the overvoltage protection when V_{5V_IN} rises above 5.42 V.

When the external OVP circuit components are connected, the SPM10140 is no longer able to coldstart from the 5 V supply input. However, if detecting a suitable 5 V power supply on 5V_IN through 5V_MON pin, the SPM10140 will coldstart from the energy on STO (if $V_{STO} \geq 1.50$ V), allowing to exit RESET STATE and then using 5V_EN to enable the charge from the 5 V power supply as explained above.

If the overvoltage protection is not needed, 5V_IN can be directly connected to the 5 V supply (keeping R_{5VIN} and C_{5VIN} is recommended), 5V_EN shall be left floating, and 5V_MON connected to GND.

5.6.3. Watchdog Timers

The SPM10140 features two watchdog timers that can be used to cut off the 5 V charger after a configured time limit:

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- The pre-charge timer is used (if enabled) when the storage element voltage (V_{STO}) is below V_{OVDIS}.
  - It starts when the 5 V charger starts charging the storage element while $V_{STO} < V_{OVDIS}$.
  - It stops when $V_{STO} \geq V_{OVDIS}$, or when the charger is disconnected or disabled through I²C.
- The CC/CV timer is used (if enabled) when the storage element voltage (V_{STO}) is greater than or equal to V_{OVDIS}.
  - It starts when the 5 V charger starts charging the storage element while $V_{STO} \geq V_{OVDIS}$.
  - It stops when the termination current $I_{5V,CV,MIN}$ is detected, or when the charger is disconnected or disabled through I²C.

Both timers are paused if the 5 V charger stops charging due to the overvoltage protection (OVP) circuit or when outside of the charging temperature range.

If any of the timers reaches its configured timeout, the 5 V charger is automatically disabled until the charger gets disconnected and then reconnected.

See Section 6.4.2 for the 5 V charger timers configuration.

5.7. IRQ Pin

The IRQ pin allows the application circuit to be notified of various events occurring in the SPM10140 (rising edge on the IRQ pin). At startup, the only event that is enabled is I2CRDY, signaling that the SPM10140 has finished to coldstart and thus, is out from RESET STATE. Other events can be enabled by writing the IRQEN0 and IRQEN1 registers (see Section 9.9).

When the IRQ pin shows a rising edge, the event that triggered it can be determined by reading the IRQFLG0 and IRQFLG1 registers (see Section 9.10). The IRQ pin is reset when the corresponding IRQFLGx register is read.

5.8. Shipping Mode

The shipping mode feature allows to force the SPM10140 in RESET STATE (see Figure 9 and Section 5.9.1), thus, disabling all SPM10140 functionalities including the buck converter and the I²C interface. The storage element is no longer charging or discharging.

The SHIP_MODE pin is monitored continuously and cannot be left floating.

The SPM10140 exits shipping mode if:

- the 5 V charger is plugged in while SHIP_MODE pin is HIGH (shipping mode enabled) and as long as the 5 V charger remains connected,
- the SHIP_MODE pin is toggled from HIGH to LOW. In this case, the SPM10140 coldstarts from the energy on STO and waits for the storage element voltage to rise up to $V_{OVDIS,BUCK}$ (or V_{OVDIS} if the buck converter is disabled), then, the SPM10140 ignores SHIP_MODE state during $T_{SHIP,IGNORE}$ (see Table 7) and goes directly into SUPPLY STATE, leaving the time for the application to startup and to force SHIP_MODE pin LOW. After $T_{SHIP,IGNORE}$, if the SHIP_MODE pin is HIGH, the SPM10140 goes back to shipping mode.

See Section 6.6 for shipping mode configuration.

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5.9. State Machine Description

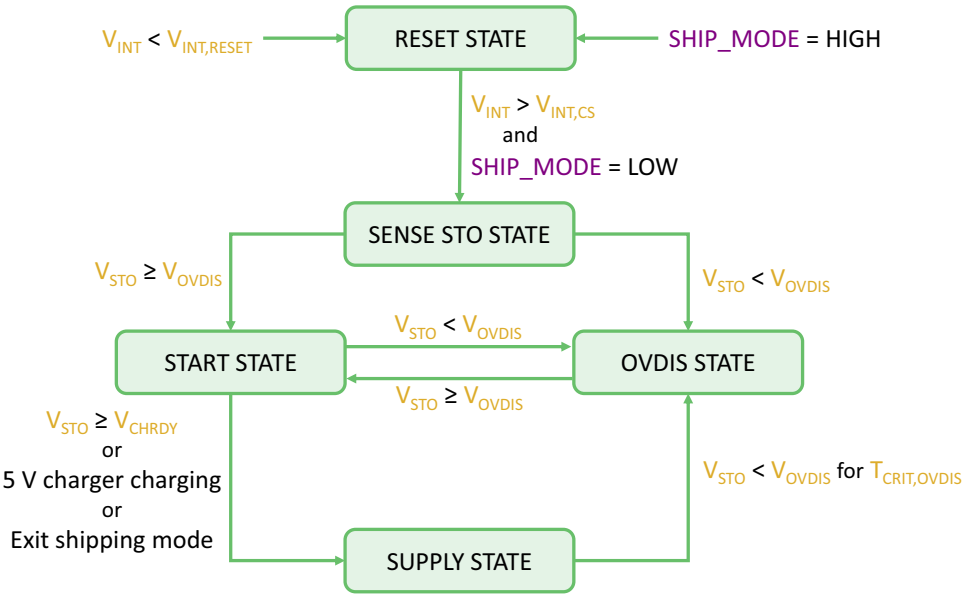


Figure 9: State machine

5.9.1. RESET STATE

The SPM10140 enters RESET STATE if one of the following is true:

- V_{INT} is below $V_{INT,RESET}$ (see Table 9).
- Shipping mode is enabled (SHIP_MODE is HIGH).

In RESET STATE, the SPM10140 behaves as follows:

- The buck converter is disabled.
- The SPM10140 internal supply (VINT) energy is provided by 5V_IN.
- Only $I_{Q,RESET}$ is drawn from the storage element connected to STO.
- ST_STO is LOW.

The SPM10140 stays in RESET STATE until the cold-start requirements (see Section 5.1) are available long enough to make V_{INT} reach $V_{INT,CS}$ (see Table 6 and Table 9). Then:

- If shipping mode is disabled (SHIP_MODE is LOW), the SPM10140 reads the value on all configuration pins and switches to SENSE STO STATE.
- If shipping mode is enabled (SHIP_MODE is HIGH), the SPM10140 stays in RESET STATE until shipping mode is disabled by setting SHIP_MODE LOW.

Please note that, from any state, the SPM10140 will switch to RESET STATE if V_{INT} drops below $V_{INT,RESET}$.

5.9.2. SENSE STO STATE

In SENSE STO STATE, the SPM10140 behaves as follows:

- A first measure of V_{STO} is performed by the SPM10140.
- The buck converter remains disabled.
- ST_STO is LOW.

The SENSE STO STATE lasts for about 2 ms.

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From SENSE STO STATE, the SPM10140 switches to:

- START STATE if $V_{STO} \geq V_{OVDIS}$.
- OVDIS STATE if $V_{STO} < V_{OVDIS}$.

From this point, the I²C interface is available (see Section 6.1.2).

5.9.3. START STATE

When in SENSE STO STATE, the SPM10140 switches to START STATE if V_{STO} is equal or higher than V_{OVDIS}.

In START STATE, the SPM10140 behaves as follows:

- The storage element connected to STO is charged from 5V_IN (if a proper power supply is connected, see Section 5.6).
- VINT internal supply energy is provided by the storage element regardless of the power available on 5V_IN.
- The buck converter (LOAD) is disabled.
- ST_STO is LOW.

From START STATE, the SPM10140 switches to:

- SUPPLY STATE if one of the following is true:
  - $V_{STO} \geq V_{CHRDY}$.
  - the 5 V charger is charging.
  - the SPM10140 has previously entered START STATE due to exiting the shipping mode (see Section 5.8).
- OVDIS STATE if $V_{STO} < V_{OVDIS}$.

5.9.4. SUPPLY STATE

When in START STATE, the SPM10140 switches to SUPPLY STATE if V_{STO} is equal or higher than V_{CHRDY}, if the 5 V charger is charging, or if the SPM10140 entered START STATE due to exiting the shipping mode.

In SUPPLY STATE, the SPM10140 behaves the same as when in START STATE, with the following differences:

- The LOAD is supplied by the buck converter if all of the following conditions are true:
  - The buck converter has been enabled by the user (see Section 6.3).
  - V_{STO} is above $V_{OVDIS,BUCK}$ (if the 5 V charger is charging) or above $V_{CHRDY,BUCK}$ (if the 5 V charger is not charging).
  - V_{STO} is above $V_{OVDIS,BUCK}$ and the SPM10140 has previously entered START STATE due to exiting the shipping mode.
  - The temperature is within the configured storage element discharge temperature range (TEMPCOLDDIS and TEMPHOTDIS, see Section 9.7).
- ST_STO is HIGH.
- If $V_{STO} \geq V_{OVCH}$, the charge of the storage element is disabled. The charge is resumed when V_{STO} drops below $V_{OVCH,LOW}$.
- If the temperature is out of the charging temperature range, the charge of the storage element is disabled. The charge is resumed when the temperature is back into the charging temperature range.

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From SUPPLY STATE, the SPM10140 sets ST_STO LOW and schedules to switch to OVDIS STATE if $V_{STO} < V_{OVDIS}$ for $T_{CRIT,ST}$. The SPM10140 then waits for the end of $T_{CRIT,OVDIS}$ to actually switch to OVDIS STATE. If V_{STO} recovers above V_{OVDIS} after $T_{CRIT,ST}$ but before the end of $T_{CRIT,OVDIS}$, the SPM10140 will still enter OVDIS STATE at the end of $T_{CRIT,OVDIS}$.

5.9.5. OVDIS STATE

The SPM10140 switches to OVDIS STATE if:

- V_{STO} is below V_{OVDIS} when in SENSE STO STATE or START STATE.
- V_{STO} remains below V_{OVDIS} for more than $T_{CRIT,ST}$ when in SUPPLY STATE (waiting for the end of $T_{CRIT,OVDIS}$ to actually switch).

In OVDIS STATE, the SPM10140 behaves as follows:

- The storage element connected to STO is charged by the 5 V charger, until either V_{STO} rises above V_{OVDIS} or V_{INT} drops below $V_{INT,RESET}$ (if the temperature is in the charging temperature range).
- VINT internal supply energy is provided by 5V_IN.
- The buck converter (LOAD) is disabled.
- ST_STO is LOW.

From OVDIS STATE, the SPM10140 switches to:

- START STATE if V_{STO} rises above V_{OVDIS}.
- RESET STATE if not enough power is available on 5V_IN to maintain V_{INT} above $V_{INT,RESET}$. In this case, the STO pin is set to high impedance, so that virtually no current is drawn from the storage element connected to STO ($I_{Q,RESET}$ as defined in Section 3.4).

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6. System Configuration

6.1. Configuration Pins and I²C

6.1.1. Configuration Pins

After a cold start, the SPM10140 reads the configuration pins. Those are then read periodically every $T_{GPIO,MON}$. The configuration pins can be changed on-the-fly. The floating configuration pins are read as HIGH, except for the SHIP_MODE pin, which cannot be left floating.

NOTE: all the I²C read-only registers (with addresses from IRQFLG0/0x13) can be read and contain valid data even if the SPM10140 is configured through GPIO. The only exception is the APM-related registers that are no longer updated when using the GPIO configuration.

6.1.2. Configuration by I²C

To configure the SPM10140 through the I²C interface after a cold start, the user must wait for the IRQ pin to rise, showing that the SPM10140 is out of RESET STATE and is ready to communicate with I²C. Please note that the IRQ pin is always low during RESET STATE. See Section 5.7 for further informations about the IRQ pin.

Once the above procedure is done, the user can write to the desired registers and validate the configuration by setting the CTRL.UPDATE register field. All configuration pins are then ignored (except the SHIP_MODE pin) and all configurations are set by the register values. All registers have a default value that can be found in Table 18.

Registers are stored in a volatile memory, so their value is lost when the SPM10140 switch to RESET STATE (due to VINT dropping below the reset voltage $V_{INT,RESET}$). The I²C communication bus reference voltage is V_{LOAD}. Once registers are written, register values are kept whether LOAD is supplied or not.

6.2. Storage Element Protection Thresholds

The storage element protection thresholds, hysteresis voltage, and temperature thresholds (explained in Section 5.3) are configurable to match various storage element types.

If the GPIO configuration is used, the STO_CFG pin allows configuring between two sets of thresholds (see Tables 11, 12, and 14).

Configuration pin	Overdischarge voltage [V]	Charge-ready voltage [V]	Overcharge voltage [V]	Storage element type
STO_CFG	V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
L	2.50	2.60	3.80	Lithium-ion Super Capacitor (LiC)
H	3.00	3.20	4.15	Lithium-ion Battery

Table 11: Storage element thresholds configuration with STO_CFG pin

Configuration pin	Buck charge-ready voltage [V]			Storage element type
STO_CFG	$V_{CHRDY,BUCK}$ for V_{LOAD} = 2.20 V	$V_{CHRDY,BUCK}$ for V_{LOAD} = 2.80 V	$V_{CHRDY,BUCK}$ for V_{LOAD} = 3.30 V	
L	2.60	2.90	3.40	Lithium-ion Super Capacitor (LiC)
H	3.20	3.20	3.50	Lithium-ion Battery

Table 12: Buck charge-ready threshold configuration with STO_CFG pin

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Configuration pin	Overcharge hysteresis [mV]	Storage element type
STO_CFG	V_{HYST}	
L	0	Lithium-ion Super Capacitor (LiC)
H	37.5	Lithium-ion Battery

Table 13: Storage element overcharge hysteresis configuration with STO_CFG pin

Configuration pin	Minimum charging temperature [°C]	Maximum charging temperature [°C]	Minimum discharging temperature [°C]	Maximum discharging temperature [°C]
STO_CFG	TEMPCOLDCH	TEMPHOTCH	TEMPCOLDDIS	TEMPHOTDIS
L	-15	60	-15	60
H	0	45	0	45

Table 14: Temperature thresholds configuration with STO_CFG pin with the recommended R_{DIV} and R_{TH}

DISCLAIMER: Storage element protection thresholds and temperature thresholds provided for each storage element type in the tables above are indicative. They are provided as is to the best knowledge of e-peas's application laboratory. They should not replace the actual values provided in the storage element manufacturer's specifications and datasheet.

The storage element buck overdischarge threshold $V_{OVDIS,BUCK}$ is not configurable. This voltage threshold is defined with the following formula:

$$V_{OVDIS,BUCK} = MAX(V_{OVDIS}, V_{LOAD})$$

If the I²C configuration is used, the following registers must be individually configured:

- VOVDIS, VCHRDY, and VOVCH: to configure the storage element protection voltage thresholds V_{OVDIS}, V_{CHRDY}, and V_{OVCH} (see Section 9.2).
- VCHRDYBUCK: to configure the buck charge-ready voltage threshold $V_{CHRDY,BUCK}$ (see Section 9.2.3).
- STOHYST: to configure the storage element overcharge hysteresis V_{HYST} (see Section 9.2.5).
- TEMPCOLDCH, TEMPHOTCH, TEMPCOLDDIS, TEMPHOTDIS, and TEMPPROTECT: to configure the storage element protection temperature thresholds (see Sections 9.6 and 9.7).

For the configuration of the voltage protection thresholds via I²C, ensure that the constraints described in Section 9.2 are respected.

For the configuration of the temperature protection thresholds via I²C, ensure that the constraints described in Section 9.5 are respected.

6.3. Load Voltage

The regulated voltage on LOAD output can be configured with the LOAD_CFG[1:0] pins (see Table 15), or through the BUCKCFG register (see Section 9.3).

Configuration pins		LOAD voltage [V]
LOAD_CFG[1:0]		V_{LOAD}
L	L	LOAD disabled
L	H	2.20
H	L	2.80
H	H	3.30

Table 15: LOAD voltage configuration with LOAD_CFG[1:0] pins

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6.4. 5 V Charger

6.4.1. Charging Current

As explained in Section 5.6.1, the SPM10140 5 V charger implements a CC/CV mode.

When in constant current (CC), the charging current $I_{5V,CC}$ is defined thanks to R_{5V_IMAX} connected between 5V_IMAX and GND, with the following formula:

$$I_{5V,CC} = \frac{60}{R_{5V_IMAX}}$$

R_{5V_IMAX} must be chosen so that $I_{5V,CC}$ complies with the range defined in Table 6. The following table provides example values of R_{5V_IMAX} with the corresponding $I_{5V,CC}$:

Resistor Ω	Maximum charging current [mA]
R_{5V_IMAX}	$I_{5V,CC}$
1200	50
400	150
150	400

Table 16: Typical resistor values for 5 V charger current configuration

Based on the configured maximum charging current $I_{5V,CC}$, the constant voltage (CV) termination current is automatically set to 10 % of $I_{5V,CC}$.

When the storage element voltage (V_{STO}) is below V_{OVDIS}, the charging current is limited to $I_{5V,OVDIS,CC}$ (see Table 6).

6.4.2. Watchdog Timers

When the SPM10140 is configured through GPIO, both 5 V charger watchdog timers are enabled. The CC/CV timer ($T_{CC/CV,TMR}$) is fixed to 10 hours, while the pre-charge timer ($T_{PRE,TMR}$) depends on STO_CFG:

Configuration pin	Pre-charge timer duration [min]
STO_CFG	$T_{PRE,TMR}$
L	120
H	30

Table 17: Pre-charge timer duration configuration with STO_CFG pin

Both timers can be enabled, disabled and configured through the CHG5V I²C register (see Section 9.4).

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6.5. Thermal Monitoring

When the thermal monitoring is enabled by connecting R_{DIV} and R_{TH} as shown in Figure 10, the SPM10140 monitors the temperature periodically every $T_{TEMP,MON}$.

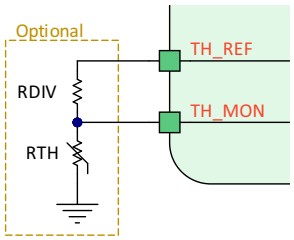


Figure 10: TH_REF and TH_MON connections

With the thermal monitoring enabled, the thermal protection can be used based on the temperature protection thresholds (see Section 6.5.1). If the thermal protection is not needed, it can be disabled through TEMPPROTECT register (see Section 9.5). In that case, if R_{DIV} and R_{TH} remain connected, the temperature will continue to be measured periodically every $T_{TEMP,MON}$ but the protection thresholds will be ignored. The temperature data remains available through the TEMP register.

If TH_MON is connected to VINT and TH_REF left floating, the thermal monitoring and thermal protections will be disabled.

6.5.1. Temperature Protection Thresholds

Once the thermal monitoring is enabled, the thermal protection can be used based on the configured temperature thresholds for charge and discharge (except if disabled by the TEMPPROTECT.EN field through I²C):

- With GPIO configuration, the typical values of R_{DIV} and R_{TH}, found in Table 10, allow for having the default temperature thresholds based on STO_CFG configuration as shown in Table 14.
- With I²C configuration, the temperature protection thresholds for storage element charge and discharge must be set individually (see Section 9.6 and 9.7), the TEMPCOLDCH, TEMPHOTCH, TEMPCOLDDIS, and TEMPHOTDIS registers can be used along with the following equations:

$$\text{THRESH}(T) = \frac{256 \times R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

$$R_{TH}(T) = R0 \times e^{B \times \left(\frac{1}{T} - \frac{1}{T_0}\right)}$$

$$T = \frac{B}{\ln\left(\frac{R_{TH}(T)}{R0}\right) + \frac{B}{T_0}}$$

- THRESH is the unsigned 8-bit value to be written in the registers to set the temperature threshold to the temperature T [K].
- R0 [Ω] is the resistance of the NTC thermistor at ambient temperature T_0 = 298.15 K (25 °C).
- $R_{TH}(T)$ [Ω] is the resistance of the thermistor at temperature T [K].
- T_0 [K] = 298.15 K (25 °C)
- T [K] is the current ambient temperature of the circuit.
- B is the characteristic constant of the thermistor, allowing to determine the resistance of the thermistor for a given temperature.

Please note that the thermistor must be of the NTC (Negative Temperature Coefficient) type. Thus, the voltage on TH_MON is inversely proportional to the temperature. This means that the value to write in the THRESH fields increases when the expected temperature threshold decreases.

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6.5.2. Temperature Hysteresis

When the thermal protection is used, a temperature hysteresis allows to avoid state toggling due to a temperature oscillating around one of the temperature thresholds.

This hysteresis behavior explained below is the same for both the charge and discharge temperature ranges.

For the cold thresholds, when the SPM10140 detects a temperature below the configured cold threshold (TEMPCOLDCH or TEMPCOLDDIS registers), the SPM10140 directly stops the charge or discharge of the storage element. The SPM10140 then waits for the temperature to rise above the cold threshold plus the hysteresis before enabling back the charge or discharge of the storage element.

For the hot thresholds, when the SPM10140 detects a temperature above the configured hot threshold (TEMPHOTCH or TEMPHOTDIS registers), the SPM10140 directly stops the charge or discharge of the storage element. The SPM10140 then waits for the temperature to drop below the hot threshold minus the hysteresis before enabling back the charge or discharge of the storage element.

The hysteresis is a number of ADC steps to add or subtract from the configured THRESH fields of the cold and hot thresholds for charge and discharge temperature ranges. One ADC step is equivalent to a voltage step of $V_{ADC,STEP}$ (see Table 9):

- With GPIO configuration, the hysteresis is fixed to 5 ADC steps (19.5 mV).
- With I²C configuration, the hysteresis is configurable through the TEMPPROTECT.HYST register field (see Section 9.5).

As explained in Section 6.5.1, the temperature ADC measurement through the thermal monitoring is inversely proportional to the temperature. This means that the cold threshold register field value is higher than the hot threshold register field value. Thus, the hysteresis is subtracted from the cold thresholds and added to the hot thresholds, as shown on the Figure 11. The hysteresis configuration must respect the constraints explained in Section 9.5.

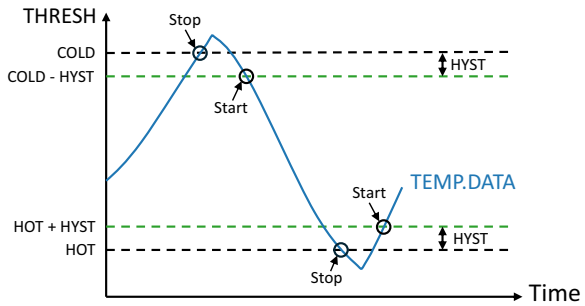


Figure 11: Thermal protection hysteresis

6.6. Shipping Mode

The shipping mode, described in Section 5.8, behaves as follows:

- Shipping mode enabled by connecting the SHIP_MODE pin to STO.
- Shipping mode disabled by connecting the SHIP_MODE pin to GND.
- A toggling from HIGH to LOW on the SHIP_MODE pin triggers a cold start from the energy stored on STO (only if $V_{STO} \geq 1.50$ V).

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7. I²C Serial Interface Protocol

The SPM10140 uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (SDA) and a serial clock line (SCL). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

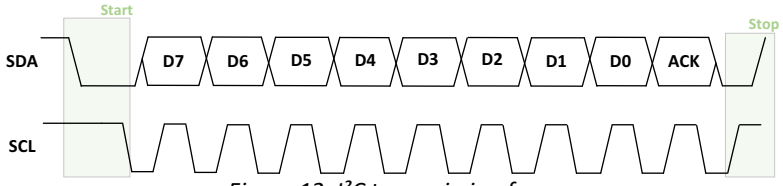


Figure 12: I²C transmission frame

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The SPM10140 is a slave that will receive configuration data or send the informations requested by the master.

The SPM10140 supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data is sent with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled-up (SDA and SCL are open drain outputs);
- Start bit (S): to initiates the transmission, the master switches the SDA line low while keeping SCL high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the SDA line from low to high while keeping SCL high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches SDA low;
- NACK: when the device receiving data keeps SDA high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x31 for the SPM10140.
- Bit [0] is the communication mode: 1 for ‘read mode’ (used when the master reads informations from the slave) and 0 for ‘write mode’ (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

Here is the procedure for the master to write a slave register:

- Master sends the address of the slave in ‘write’ mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the VOVCH register, the master sends the value 0x04;
- Slave sends an ACK;
- Master sends the data to write to the register;

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- Slave sends an ACK;
- If the master wants to write register at the next address (STOHYST in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several consecutive registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the IRQFLG0 register, the master sends the value 0x13;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in 'read' mode;
- Slave sends an ACK;
- Master provides the clock on SCL to allow the slave to shift the data of the read register on SDA;
- If the master wants to read register at the next address (IRQFLG1 in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for reading several registers;
- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in Figure 13. Refer to Table 18 for all register addresses.

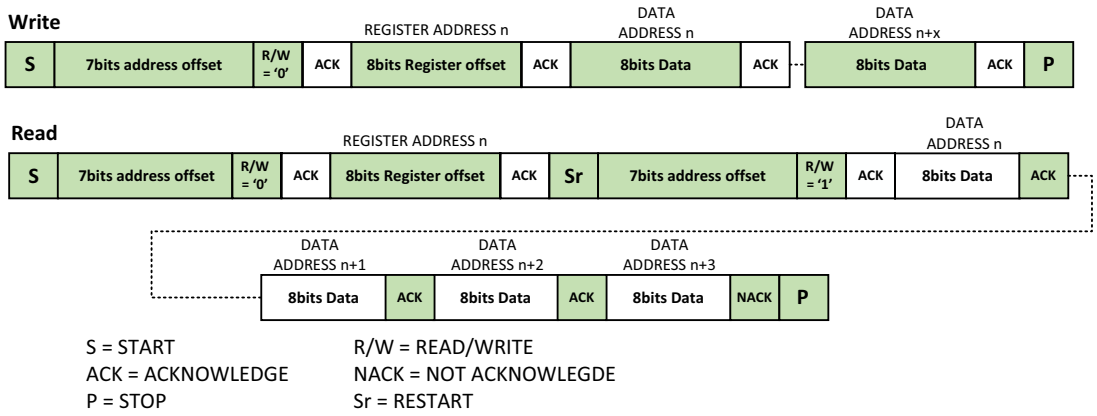


Figure 13: Read and write I²C transmission

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8. Register Map

Please note that the SPM10140 device address is 0x31.

Address	Name	Bit	Field Name	Access	Reset	Description
0x02	VOVDIS	[4:0]	THRESH	R/W	0x04	STO overdischarge threshold.
0x03	VCHRDY	[4:0]	THRESH	R/W	0x04	STO charge-ready threshold.
0x04	VOVCH	[5:0]	THRESH	R/W	0x16	STO overcharge threshold.
0x05	STOHYST	[1:0]	VHYST	R/W	0x00	STO hysteresis configuration.
0x06	RSVD	-	-	-	-	Reserved (write-ignore).
0x07	BUCKCFG	[0:0]	EN	R/W	0x00	Buck converter enable.
		[2:1]	VLOAD	R/W	0x00	LOAD voltage configuration.
		[3:3]	BYPASSEN	R/W	0x00	Buck converter bypass mode enable.
0x08	VCHRDYBUCK	[4:0]	THRESH	R/W	0x04	STO charge-ready buck threshold.
0x09	CHG5V	[0:0]	EN	R/W	0x01	5 V charger enable.
		[1:1]	TMREN	R/W	0x01	Watchdog timers enable.
		[3:2]	PRETMRCFG	R/W	0x00	Pre-charge timer configuration.
		[5:4]	CCCVTMRCFG	R/W	0x00	CC/CV timer configuration.
0x0A	TEMPCOLDCH	[7:0]	THRESH	R/W	0xB9	Cold temperature threshold for storage element charging.
0x0B	TEMPHOTCH	[7:0]	THRESH	R/W	0x1F	Hot temperature threshold for storage element charging.
0x0C	TEMPCOLDDIS	[7:0]	THRESH	R/W	0xB9	Cold temperature threshold for storage element discharging.
0x0D	TEMPHOTDIS	[7:0]	THRESH	R/W	0x1F	Hot temperature threshold for storage element discharging.
0x0E	TEMPPROTECT	[0:0]	EN	R/W	0x01	Thermal protection enable.
		[3:1]	HYST	R/W	0x05	Thermal protection hysteresis configuration.
0x0F	APM	[0:0]	-	-	-	Reserved (write-ignore).
		[1:1]	LOADEN	R/W	0x00	APM LOAD enable.
0x10	IRQEN0	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable.
		[1:1]	VOVDIS	R/W	0x00	IRQ VOVDIS enable.
		[2:2]	VCHRDY	R/W	0x00	IRQ VCHRDY enable.
		[3:3]	VOVCH	R/W	0x00	IRQ VOVCH enable.
		[4:4]	-	-	-	Reserved (write-ignore).
		[5:5]	TEMPCH	R/W	0x00	IRQ temperature charge enable.
		[6:6]	TEMPDIS	R/W	0x00	IRQ temperature discharge enable.
		[7:7]	LOADSHTDWN	R/W	0x00	IRQ LOAD shutdown enable.
0x11	IRQEN1	[1:0]	-	-	-	Reserved (write-ignore).
		[2:2]	STODONE	R/W	0x00	IRQ STO measurement done enable.
		[3:3]	TEMPDONE	R/W	0x00	IRQ temperature measurement done enable.
		[4:4]	APMDONE	R/W	0x00	IRQ APM done enable.
		[5:5]	APMERR	R/W	0x00	IRQ APM error enable.
		[6:6]	CHG5VCONN	R/W	0x00	IRQ 5 V charger connected enable.
		[7:7]	CHG5VON	R/W	0x00	IRQ 5 V charger ON enabled.

Table 18: Register map (part 1)

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Address	Name	Bit	Field Name	Access	Reset	Description
0x12	CTRL	[0:0]	UPDATE	R/W	0x00	Load I²C registers configuration.
		[1:1]	-	-	-	Reserved.
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag.
0x13	IRQFLG0	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag.
		[1:1]	VOVDIS	R	0x00	IRQ VOVDIS flag.
		[2:2]	VCHRDY	R	0x00	IRQ VCHRDY flag.
		[3:3]	VOVCH	R	0x00	IRQ VOVCH flag.
		[4:4]	-	-	-	Reserved.
		[5:5]	TEMPCH	R	0x00	IRQ temperature (charge) flag.
		[6:6]	TEMPDIS	R	0x00	IRQ temperature (discharge) flag.
		[7:7]	LOADSHTDWN	R	0x00	IRQ LOAD shutdown flag.
0x14	IRQFLG1	[1:0]	-	-	-	Reserved.
		[2:2]	STODONE	R	0x00	IRQ STO measurement done flag.
		[3:3]	TEMPDONE	R	0x00	IRQ temperature measurement done flag.
		[4:4]	APMDONE	R	0x00	IRQ APM done flag.
		[5:5]	APMERR	R	0x00	IRQ APM error flag.
		[6:6]	CHG5VCONN	R	0x00	IRQ 5 V charger connected flag.
		[7:7]	CHG5VON	R	0x00	IRQ 5 V charger ON flag.
0x15	STATUS0	[0:0]	OVDIS	R	0x00	Status overdischarge.
		[1:1]	CHRDY	R	0x00	Status charge-ready.
		[2:2]	OVCH	R	0x00	Status overcharge.
		[3:3]	-	-	-	Reserved.
		[4:4]	CHG5VCONN	R	0x00	Status 5 V charger connected.
		[5:5]	CHG5VON	R	0x00	Status 5 V charger ON.
0x16	STATUS1	[0:0]	TEMPCOLDCH	R	0x00	Status cold temperature (charge).
		[1:1]	TEMPHOTCH	R	0x00	Status hot temperature (charge).
		[2:2]	TEMPCOLDDIS	R	0x00	Status cold temperature (discharge).
		[3:3]	TEMPHOTDIS	R	0x00	Status hot temperature (discharge).
0x17 ... 0x19	-	-	-	-	-	Reserved.
0x1A	APM0LOAD	[7:0]	DATA	R	0x00	APM data 0 (LOAD).
0x1B	APM1LOAD	[7:0]	DATA	R	0x00	APM data 1 (LOAD).
0x1C	APM2LOAD	[7:0]	DATA	R	0x00	APM data 2 (LOAD).
0x1D	APMERR	[0:0]	-	-	-	Reserved.
		[1:1]	LOADERR	R	0x00	APM LOAD corrupted.
0x1E	TEMP	[7:0]	DATA	R	0x00	Temperature monitoring value.
0x1F	STO	[7:0]	DATA	R	0x00	STO monitoring value.

Table 18: Register map (part 2)

NOTE: The SPM10140 shares a common register map with the AEM11920 and AEM11921. With the exception of some reserved registers that can be written with no effect on the device, the register addresses, bit definitions, and default values are identical, allowing the use of shared software drivers.

NOTE: The reserved registers marked as "write-ignore" can safely be written with any value and has no effect on the SPM10140 behavior, allowing the user to write all the registers at once, as described in Section 7.

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9. Registers Configuration

9.1. I²C Control (CTRL)

The CTRL register allows for updating the SPM10140 configurations and checking registers synchronization status.

CTRL register	Address: 0x12	Access: R/W	Reset: 0x00
Bit [7:3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	SYNCBUSY	RESERVED	UPDATE
-	0x00	-	0x00

Table 19: CTRL register

Bit [2]: system registers synchronization (CTRL.SYNCBUSY)

This field indicates whether the synchronization from the I²C registers to the system registers is ongoing or not.

- 0: CTRL register not synchronizing.
- 1: CTRL register synchronizing.

Bit [0]: system registers update (CTRL.UPDATE)

This field is used to control the source of the SPM10140 configurations (GPIO or I²C) and to update the configurations with the current I²C register values or GPIO states.

- 0: GPIO
  - W: load configurations from the GPIO.
  - R: configurations from the GPIO is currently used if read as 0.
- 1: I2C
  - W: load configurations from the I²C registers.
  - R: configurations from the I²C registers is currently used if read as 1.

NOTE: if the SPM10140 is already configured through the I²C registers, writing any register does not have any effect until 1 is written to the CTRL.UPDATE field, leading to the SPM10140 to read the new register values and apply them.

NOTE: when using I²C register configuration, the user can switch back to GPIO configuration by writing 0 to the CTRL.UPDATE field. In that case, the settings previously written and applied to the IRQEN registers are maintained even when using GPIO configuration, as well as the data in IRQFLG register.

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9.2. Storage Element Threshold Voltages

The storage element protection thresholds, described in Section 5.3, can be set independently by the registers VOVDIS, VCHRDY, VCHRDYBUCK, VOVCH, and STOHYST.

For the configuration of those thresholds, please always respect the following constraints to ensure the functionality of the SPM10140:

- V_{OVDIS} + 100 mV < V_{CHRDY}
- $V_{CHRDY} \leq V_{CHRDY,BUCK}$
- $V_{OVDIS,BUCK} < V_{CHRDY,BUCK}$
- $V_{CHRDY,BUCK} < V_{OVCH,LOW}$
- $V_{CHRDY,BUCK} \geq V_{LOAD}$
- V_{CHRDY} + 100 mV < V_{OVCH}

9.2.1. Overdischarge Voltage (VOVDIS)

The VOVDIS register allows the configuration of the storage element voltage below which the storage element is considered to be fully depleted, and must not be discharged any further (V_{OVDIS}).

VOVDIS register	Address: 0x02	Access: R/W	Reset: 0x04
Bit [7:5]		Bit [4:0]	
RESERVED		THRESH	
-		0x04	

Table 20: VOVDIS register

Bit [4:0]: storage element overdischarge threshold (VOVDIS.THRESH)

This field allows the configuration of V_{OVDIS} based on Table 21 values or based on the following formula:

$$V_{OVDIS} = MIN(3.5; 2.3 + THRESH \times 0.05)$$

VOVDIS. THRESH	V_{OVDIS} [V]	VOVDIS. THRESH	V_{OVDIS} [V]	VOVDIS. THRESH	V_{OVDIS} [V]
0x00	2.30	0x09	2.75	0x12	3.20
0x01	2.35	0x0A	2.80	0x13	3.25
0x02	2.40	0x0B	2.85	0x14	3.30
0x03	2.45	0x0C	2.90	0x15	3.35
0x04	2.50	0x0D	2.95	0x16	3.40
0x05	2.55	0x0E	3.00	0x17	3.45
0x06	2.60	0x0F	3.05	0x18	3.50
0x07	2.65	0x10	3.10	...	
0x08	2.70	0x11	3.15	0x1F	

Table 21: Storage element V_{OVDIS} configuration by VOVDIS register

CAUTION: For VOVDIS.THRESH configuration, always respect the constraints described in Section 9.2.

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9.2.2. Charge-Ready Voltage (VCHRDY)

The VCHRDY register allows the configuration of the storage element charge-ready voltage (V_{CHRDY}) required to switch to SUPPLY STATE when the 5 V charger is not charging and if the SPM10140 has not just exited shipping mode (see Section 5.3).

VCHRDY register	Address: 0x03	Access: R/W	Reset: 0x04
Bit [7:5]		Bit [4:0]	
RESERVED		THRESH	
-		0x04	

Table 22: VCHRDY register

Bit [4:0]: storage element charge-ready threshold (VCHRDY.THRESH)

This field allows the configuration of V_{CHRDY} based on Table 23 values or based on the following formula:

$$V_{CHRDY} = MIN(3.6; 2.4 + THRESH \times 0.05)$$

VCHRDY. THRESH	V_{CHRDY} [V]	VCHRDY. THRESH	V_{CHRDY} [V]	VCHRDY. THRESH	V_{CHRDY} [V]
0x00	2.40	0x09	2.85	0x12	3.30
0x01	2.45	0x0A	2.90	0x13	3.35
0x02	2.50	0x0B	2.95	0x14	3.40
0x03	2.55	0x0C	3.00	0x15	3.45
0x04	2.60	0x0D	3.05	0x16	3.50
0x05	2.65	0x0E	3.10	0x17	3.55
0x06	2.70	0x0F	3.15	0x18	3.60
0x07	2.75	0x10	3.20	...	
0x08	2.80	0x11	3.25	0x1F	

Table 23: Storage element V_{CHRDY} configuration by VCHRDY register

CAUTION: For VCHRDY.THRESH configuration, always respect the constraints described in Section 9.2.

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9.2.3. Buck Charge-Ready Voltage (VCHRDYBUCK)

The VCHRDYBUCK register allows the configuration of the storage element voltage ($V_{CHRDY,BUCK}$) at which the buck converter can be enabled when the 5 V charger is not used (see Section 5.3).

VCHRDYBUCK register	Address: 0x08	Access: R/W	Reset: 0x04
Bit [7:5]		Bit [4:0]	
RESERVED		THRESH	
-		0x04	

Table 24: VCHRDYBUCK register

Bit [4:0]: storage element buck charge-ready threshold (VCHRDYBUCK.THRESH)

This field allows the configuration of the storage element buck charge-ready threshold. This voltage threshold is then used to check if the buck converter can be enabled or if the storage element voltage is still too low (when the 5 V charger is not used).

The buck charge-ready voltage can be determined based on Table 25 or on the following formula:

$$V_{CHRDY,BUCK} = \mathrm{MIN}(3.6;\ 2.4 + \mathrm{THRESH} \times 0.05)$$

VCHRDYBUCK .THRESH	$V_{CHRDY,BUCK}$ [V]	VCHRDYBUCK .THRESH	$V_{CHRDY,BUCK}$ [V]	VCHRDYBUCK .THRESH	$V_{CHRDY,BUCK}$ [V]
0x00	2.40	0x09	2.85	0x12	3.30
0x01	2.45	0x0A	2.90	0x13	3.35
0x02	2.50	0x0B	2.95	0x14	3.40
0x03	2.55	0x0C	3.00	0x15	3.45
0x04	2.60	0x0D	3.05	0x16	3.50
0x05	2.65	0x0E	3.10	0x17	3.55
0x06	2.70	0x0F	3.15	0x18	
0x07	2.75	0x10	3.20	...	3.60
0x08	2.80	0x11	3.25	0x1F	

Table 25: Storage element $V_{CHRDY,BUCK}$ configuration by VCHRDYBUCK register

CAUTION: For VCHRDYBUCK.THRESH configuration, always respect the constraints described in Section 9.2.

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9.2.4. Overcharge Voltage (VOVCH)

The VOVCH register allows the configuration of the storage element maximum voltage before disabling its charging (V_{OVCH}).

VOVCH register	Address: 0x04	Access: R/W	Reset: 0x16
Bit [7:6]	Bit [5:0]		
RESERVED	THRESH		
-	0x16		

Table 26: VOVCH register

Bit [5:0]: storage element overcharge threshold (VOVCH.THRESH)

This field allows the configuration of V_{OVCH} based on Table 27 values or based on the following:

$$V_{OVCH} = \mathrm{MIN}(4.6;\ 2.7 + \mathrm{THRESH} \times 0.05)$$

VOVCH. THRESH	V_{OVCH} [V]	VOVCH. THRESH	V_{OVCH} [V]	VOVCH. THRESH	V_{OVCH} [V]
0x00	2.70	0x0E	3.40	0x1C	4.10
0x01	2.75	0x0F	3.45	0x1D	4.15
0x02	2.80	0x10	3.50	0x1E	4.20
0x03	2.85	0x11	3.55	0x1F	4.25
0x04	2.90	0x12	3.60	0x20	4.30
0x05	2.95	0x13	3.65	0x21	4.35
0x06	3.00	0x14	3.70	0x22	4.40
0x07	3.05	0x15	3.75	0x23	4.45
0x08	3.10	0x16	3.80	0x24	4.50
0x09	3.15	0x17	3.85	0x25	4.55
0x0A	3.20	0x18	3.90	0x26 ... 0x3F	4.60
0x0B	3.25	0x19	3.95		
0x0C	3.30	0x1A	4.00		
0x0D	3.35	0x1B	4.05		

Table 27: Storage element V_{OVCH} configuration by VOVCH register

CAUTION: For VOVCH.THRESH configuration, always respect the constraints described in Section 9.2.

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9.2.5. Storage Element Voltage Hysteresis (STOHYST)

The STOHYST register allows the configuration of the storage element hysteresis voltage (V_{HYST}). See Section 5.3.

STOHYST register	Address: 0x05	Access: R/W	Reset: 0x00
Bit [7:2]			Bit [1:0]
RESERVED			VHYST
-			0x00

Table 28: STOHYST register

Bit [1:0]: storage element hysteresis voltage (STOHYST.VHYST)

This field allows the configuration of V_{HYST} based on Table 29 to determine the storage element overcharge low threshold:

$$V_{OVCH,LOW} = V_{OVCH} - V_{HYST}$$

STOHYST		Overcharge hysteresis [mV]
VHYST		V_{HYST}
0	0	0
0	1	37.5
1	0	75
1	1	112.5

Table 29: Storage element hysteresis configuration by STOHYST register

CAUTION: For $V_{OVCH,LOW}$ configuration through STOHYST.VHYST register, always respect the constraints described in Section 9.2.

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9.3. Buck Converter (BUCKCFG)

The BUCK register allows the configuration of the buck converter output (LOAD).

BUCKCFG register	Address: 0x07	Access: R/W	Reset: 0x00
Bit [7:4]	Bit [3]	Bit [2:1]	Bit [0]
RESERVED	BYPASSEN	VLOAD	EN
-	0x00	0x00	0x00

Table 30: BUCKCFG register

Bit [3]: buck converter bypass mode enable (BUCKCFG.BYPASSEN)

This field allows enabling or disabling the buck converter bypass mode (see Section 5.2.2).

- 0: disable the bypass mode.
- 1: enable the bypass mode.

Bit [2:1]: buck converter output regulation voltage (BUCKCFG.VLOAD)

This field allows the configuration of the buck converter regulation output voltage (V_{LOAD}). The available configurations can be found in Table 31.

BUCKCFG	Buck converter output voltage [V]
VLOAD	V_{LOAD}
0x00	2.20
0x01	2.80
0x02	3.00
0x03	3.30

Table 31: V_{LOAD} settings by BUCKCFG.VLOAD register

Bit [0]: buck converter enable (BUCKCFG.EN)

This field allows enabling or disabling the buck converter (see Section 5.2).

- 0: disable the buck converter.
- 1: enable the buck converter.

CAUTION: V_{LOAD} is used as the I²C bus supply. If disabling the buck converter output (LOAD), ensure to short the LOAD pin to the STO pin or to supply it externally with a voltage less than or equal to V_{STO} in order to keep the I²C bus working (see Section 5.2).

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9.4. 5 V Charger (CHG5V)

The CHG5V register allows the configuration of the 5 V charger (as explained in Section 5.6).

CHG5V register	Address: 0x09	Access: R/W	Reset: 0x03	
Bit [7:6]	Bit [5:4]	Bit [3:2]	Bit [1]	Bit [0]
RESERVED	CCCVTMRCFG	PRETMRCFG	TMREN	EN
-	0x00	0x00	0x01	0x01

Table 32: CHG5V register

Bit [5:4]: 5 V charger CC/CV timer configuration (CHG5V.CCCVTMRCFG)

This field allows configuring the CC/CV timer duration based on Table 33 values. See Section 5.6.3 for detailed behavior of this timer.

CHG5V	CC/CV timer duration [h]
CCCVTMRCFG	$T_{CC/CV,TMR}$
0x00	2.5
0x01	5
0x02	10
0x03	20

Table 33: CC/CV timer duration configuration by CHG5V.CCCVTMRCFG register

Bit [3:2]: 5 V charger pre-charge timer configuration (CHG5V.PRETMRCFG)

This field allows configuring the pre-charge timer duration based on Table 34 values. See Section 5.6.3 for detailed behavior of this timer.

CHG5V	Pre-charge timer duration [min]
PRETMRCFG	$T_{PRE,TMR}$
0x00	15
0x01	30
0x02	60
0x03	120

Table 34: Pre-charge timer duration configuration by CHG5V.PRETMRCFG register

Bit [1]: 5 V charger watchdog timers enable (CHG5V.TMREN)

This field allows enabling or disabling the two watchdog timers (pre-charge and CC/CV) for the 5 V charger (see Section 5.6.3).

- 0: disable both timers.
- 1: enable both timers.

Bit [0]: 5 V charger enable (CHG5V.EN)

This field allows enabling or disabling the 5 V charger.

- 0: disable the 5 V charger.
- 1: enable the 5 V charger.

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9.5. Thermal Protection (TEMPPROTECT)

The TEMPPROTECT register allows enabling or disabling the thermal protection, explained in Section 6.5.1, based on the protection thresholds described in Sections 9.6 and 9.7.

To use the thermal protection, the thermal monitoring external components must be mounted as described in Section 6.5.

For the configuration of the thermal protection thresholds, please always respect the following constraints to ensure the functionality of the SPM10140 (see Figure 11):

- TEMPCOLDCH.THRESH - TEMPPROTECT.HYST > TEMPHOTCH.THRESH + TEMPPROTECT.HYST
- TEMPCOLDDIS.THRESH - TEMPPROTECT.HYST > TEMPHOTDIS.THRESH + TEMPPROTECT.HYST

TEMPPROTECT register	Address: 0x0E	Access: R/W	Reset: 0x0B
Bit [7:4]		Bit [3:1]	Bit [0]
RESERVED		HYST	EN
-		0x05	0x01

Table 35: TEMPPROTECT register

Bit [3:1]: thermal protection hysteresis (TEMPPROTECT.HYST)

This field allows the configuration of the number of ADC steps used as hysteresis for the thermal protection thresholds. The available configurations can be found in Table 36.

One ADC step is equivalent to a voltage step equal to $V_{ADC,STEP}$ (see Table 9).

Bit [0]: thermal protection monitoring enable (TEMPPROTECT.EN)

This field allows enabling or disabling the thermal protection monitoring:

- 0: disable the thermal protection.
- 1: enable the thermal protection.

TEMPPROTECT.HYST	Number of hysteresis ADC steps[1]
0x00	0
0x01	1
0x02	2
0x03	3
0x04	4
0x05	5
0x06	6
0x07	7

Table 36: Thermal hysteresis configuration by TEMPPROTECT.HYST register

1. One ADC step is equivalent to $V_{ADC,STEP}$ (see Table 9).

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9.6. Storage Element Charge Temperature Protection

The storage element charge temperature protection thresholds (TEMPCOLDCH and TEMPHOTCH) are used when the thermal monitoring is enabled with R_{DIV} and R_{TH} (see Section 6.5) and when the thermal protection (TEMPPROTECT) is enabled (see Section 9.5).

If the temperature is out of the charge temperature range defined between TEMPCOLDCH and TEMPHOTCH, the 5 V charger will be disabled to stop charging the storage element.

THRESH value is determined as follows from the desired temperature T:

- Determine the resistance of the thermo resistor R_{TH} at the desired temperature.
- Calculate THRESH using the following formula:

$$\mathrm{THRESH}(T) = \frac{256 \times R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

See Section 6.5 for further information about thermal monitoring configuration.

CAUTION: For TEMPCOLDCH and TEMPHOTCH configuration, make sure to respect the constraints described in Section 9.5.

9.6.1. TEMPCOLDCH

The TEMPCOLDCH register allows the configuration of the minimum temperature below which the charge of the storage element is disabled.

TEMPCOLDCH register	Address: 0x0A	Access: R/W	Reset: 0xB9
Bit [7:0]			
THRESH			
0xB9			

Table 37: TEMPCOLDCH register

Bit [7:0]: storage element charge minimum temperature threshold (TEMPCOLDCH.THRESH)

This field allows the configuration of the minimum temperature (cold) threshold for enabling the storage element charge.

9.6.2. TEMPHOTCH

The TEMPHOTCH register allows the configuration of the maximum temperature above which the charge of the storage element is disabled.

TEMPHOTCH register	Address: 0x0B	Access: R/W	Reset: 0x1F
Bit [7:0]			
THRESH			
0x1F			

Table 38: TEMPHOTCH register

Bit [7:0]: storage element charge maximum temperature threshold (TEMPHOTCH.THRESH)

This field allows the configuration of the maximum temperature (hot) threshold for enabling the storage element charge.

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9.7. Storage Element Discharge Temperature Protection

The storage element discharge temperature protection thresholds (TEMPCOLDDIS and TEMPHOTDIS) are used when the thermal monitoring is enabled with R_{DIV} and R_{TH} (see Section 6.5) and when the thermal protection (TEMPPROTECT) is enabled (see Section 9.5).

If the temperature is out of the discharge temperature range defined between TEMPCOLDDIS and TEMPHOTDIS, the buck converter will be disabled to stop discharging the storage element through the LOAD. In this case, VINT will continue to be supplied from STO.

THRESH value is determined as follows from the desired temperature T:

- Determine the resistance of the thermo resistor R_{TH} at the desired temperature.
- Calculate THRESH using the following formula:

$$\mathrm{THRESH}(T) = \frac{256 \times R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

See Section 6.5 for further information about thermal monitoring configuration.

CAUTION: For TEMPCOLDDIS and TEMPHOTDIS configuration, make sure to respect the constraints described in Section 9.5.

9.7.1. TEMPCOLDDIS

The TEMPCOLDDIS register allows the configuration of the minimum temperature (cold) below which the discharge of the storage element is disabled.

TEMPCOLDDIS register	Address: 0x0C	Access: R/W	Reset: 0xB9
Bit [7:0]			
THRESH			
0xB9			

Table 39: TEMPCOLDDIS register

Bit [7:0]: storage element discharge minimum temperature threshold (TEMPCOLDDIS.THRESH)

This field allows the configuration of the minimum temperature (cold) threshold for enabling the storage element discharge.

9.7.2. TEMPHOTDIS

The TEMPHOTDIS register allows the configuration of the maximum temperature (hot) above which the discharge of the storage element is disabled.

TEMPHOTDIS register	Address: 0x0D	Access: R/W	Reset: 0x1F
Bit [7:0]			
THRESH			
0x1F			

Table 40: TEMPHOTDIS register

Bit [7:0]: storage element discharge maximum temperature threshold (TEMPHOTDIS.THRESH)

This field allows the configuration of the maximum temperature (hot) threshold for enabling the storage element discharge.

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9.8. Average Power Monitoring (APM)

The APM register allows the configuration of the Average Power Monitoring feature for the LOAD APM (buck converter).

For APM feature explanations, refer to the Section 5.5. For APM data interpretation, refer to the Section 9.12.

APM register	Address: 0x0F	Access: R/W	Reset: 0x00	
Bit [7:0]			Bit [1]	Bit [0]
RESERVED			LOADEN	RESERVED
-			0x00	-

Table 41: APM register

Bit [1]: load output APM enable (APM.LOADEN)

This field allows enabling or disabling the APM for LOAD.

- 0: disable the load output APM.
- 1: enable the load output APM.

Bit [0]: Reserved write-ignore

This register field can be written with any value and has no impact on the SPM10140.

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9.9. IRQ Enable (IRQENx)

9.9.1. IRQEN0

The IRQEN0 register allows the configuration of which events trigger the IRQ pin rising edge (see also the IRQEN1 register).

IRQEN0 register		Address: 0x10		Access: R/W		Reset: 0x01	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
LOADSHTDWN	TEMPDIS	TEMPCH	RESERVED	VOVCH	VCHRDY	VOVDIS	I2CRDY
0x00	0x00	0x00	-	0x00	0x00	0x00	0x01

Table 42: IRQEN0 register

Bit [7]: buck converter output shutdown (IRQEN0.LOADSHTDWN)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.LOADSHTDWN flag when the buck converter is about to be disabled following the detection of an empty storage element or thermal shutdown (see Section 5.2).

- 0: disable the IRQ flag for LOAD shutdown.
- 1: enable the IRQ flag for LOAD shutdown.

Bit [6]: storage element discharge temperature (IRQEN0.TEMPDIS)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.TEMPDIS flag when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers).

- 0: disable the IRQ flag for discharge temperature range.
- 1: enable the IRQ flag for discharge temperature range.

Bit [5]: storage element charge temperature (IRQEN0.TEMPCH)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.TEMPCH flag when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers).

- 0: disable the IRQ flag for charge temperature range.
- 1: enable the IRQ flag for charge temperature range.

Bit [4]: Reserved write-ignore

This register field can be written with any value and has no impact on the SPM10140.

Bit [3]: storage element overcharge (IRQEN0.VOVCH)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.VOVCH flag when the storage element voltage crosses V_{OVCH} (selected through the VOVCH register).

- 0: disable the IRQ flag for V_{OVCH} crossing.
- 1: enable the IRQ flag for V_{OVCH} crossing.

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Bit [2]: storage element charge-ready (IRQEN0.VCHRDY)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.VCHRDY flag when the storage element voltage crosses V_{CHRDY} (selected through the VCHRDY register).

- 0: disable the IRQ flag for V_{CHRDY} crossing.
- 1: enable the IRQ flag for V_{CHRDY} crossing.

Bit [1]: storage element overdischarge (IRQEN0.VOVDIS)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.VOVDIS flag after $T_{CRIT,ST}$ when the storage element voltage drops below V_{OVDIS} (selected through the VOVDIS register) or directly when the storage element voltage rises above V_{OVDIS}.

- 0: disable the IRQ flag for V_{OVDIS} crossing.
- 1: enable the IRQ flag for V_{OVDIS} crossing.

Bit [0]: I2C interface ready (IRQEN0.I2CRDY)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG0.I2CRDY flag when the serial interface (I^2C) is ready to communicate.

- 0: disable the IRQ flag for I^2C interface readiness.
- 1: enable the IRQ flag for I^2C interface readiness.

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9.9.2. IRQEN1

The IRQEN1 register allows the configuration of which events trigger the IRQ pin rising edge (see also the IRQEN0 register).

IRQEN1 register		Address: 0x11		Access: R/W		Reset: 0x00
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1:0]
CHG5VON	CHG5VCONN	APMERR	APMDONE	TEMPDONE	STODONE	RESERVED
0x00	0x00	0x00	0x00	0x00	0x00	-

Table 43: IRQEN1 register

Bit [7]: 5 V charger charging (IRQEN1.CHG5VON)

This field allows enabling of disabling the generation of a rising edge on the IRQ pin with the IRQFLG1.CHG5VON flag when the 5 V charger starts or stops to charge the storage element.

- 0: disable the IRQ flag for 5 V charger charge.
- 1: enable the IRQ flag for 5 V charger charge.

Bit [6]: 5 V charger connected (IRQEN1.CHG5VCONN)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.CHG5VCONN flag when the 5 V charger gets connected or disconnected (see Table 6 for V_{5V_IN} requirements).

- 0: disable the IRQ flag for 5 V charger connection.
- 1: enable the IRQ flag for 5 V charger connection.

Bit [5]: APM error (IRQEN1.APMERR)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.APMERR flag when an APM error occurs.

- 0: disable the IRQ flag for APM errors.
- 1: enable the IRQ flag for APM errors.

Bit [4]: APM done (IRQEN1.APMDONE)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.APMDONE flag when APM data is available.

- 0: disable the IRQ flag for new available APM data.
- 1: enable the IRQ flag for new available APM data.

Bit [3]: temperature measurement done (IRQEN1.TEMPDONE)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.TEMPDONE flag when the temperature measurement is done.

- 0: disable the IRQ flag for temperature measurement completion.
- 1: enable the IRQ flag for temperature measurement completion.

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Bit [2]: storage element voltage measurement done (IRQEN1.STODONE)

This field allows enabling or disabling the generation of a rising edge on the IRQ pin with IRQFLG1.STODONE flag when the storage element voltage measurement is done.

- 0: disable the IRQ flag for STO voltage measurement completion.
- 1: enable the IRQ flag for STO voltage measurement completion.

Bit [1:0]: Reserved write-ignore

These register fields can be written with any value and have no impact on the SPM10140.

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9.10. IRQ Flags (IRQFLGx)

The IRQFLGx registers allow the user to get a status about specific SPM10140 events (along with the STATUSx registers, see Section 9.11). When the event happens, the IRQ pin switches HIGH and the register field bit that corresponds to the event will switch to 1, provided that the event flag has been enabled in the corresponding IRQENx register. The bit will stay to 1 and the IRQ pin will stay HIGH until the IRQFLGx register is read.

Please note that, while the I²C configuration must be used to enable the SPM10140 IRQ flags, the behavior of the IRQ pin as well as the IRQFLGx register stays the same even if the SPM10140 has switched back to GPIO configuration by writing 0 to CTRL.UPDATE.

9.10.1. IRQFLG0

The IRQFLG0 register is the IRQ pin event flags register 0.

IRQFLG0 register		Address: 0x13		Access: R		Reset: 0x00	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
LOADSHTDWN	TEMPDIS	TEMPCH	RESERVED	VOVCH	VCHRDY	VOVDIS	I2CRDY
0x00	0x00	0x00	-	0x00	0x00	0x00	0x00

Table 44: IRQFLG0 register

Bit [7]: buck converter output shutdown (IRQFLG0.LOADSHTDWN)

This IRQ pin event flag is set when the buck converter is about to be disabled following the detection of an empty storage element or thermal shutdown (see Section 5.2), if the corresponding event source has been previously enabled through the IRQEN0.LOADSHTDWN field.

- 0: buck converter output (LOAD) shutdown is not about to be disabled.
- 1: buck converter output (LOAD) shutdown is about to be disabled in $T_{LOAD,DIS}$ - $T_{CRIT,LOAD}$ (see Table 7).

Bit [6]: storage element discharge temperature (IRQFLG0.TEMPDIS)

This IRQ pin event flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers), if the corresponding event source has been previously enabled through the IRQEN0.TEMPDIS field.

- 0: the temperature did not cross the minimum or maximum temperature allowed for discharging.
- 1: the temperature crossed the minimum or maximum temperature allowed for discharging.

Bit [5]: storage element charge temperature (IRQFLG0.TEMPCH)

This IRQ pin event flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers), if the corresponding event source has been previously enabled through the IRQEN0.TEMPCH field.

- 0: the temperature did not cross the minimum or maximum temperature allowed for charging.
- 1: the temperature crossed the minimum or maximum temperature allowed for charging.

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Bit [3]: storage element overcharge (IRQFLG0.VOVCH)

This IRQ pin event flag is set when the storage element voltage crosses V_{OVCH} (selected through the VOVCH register), if the corresponding event source has been previously enabled through the IRQEN0.VOVCH field.

- 0: the storage element voltage did not cross V_{OVCH}.
- 1: the storage element voltage crossed V_{OVCH}.

Bit [2]: storage element charge-ready (IRQFLG0.VCHRDY)

This IRQ pin event flag is set when the storage element voltage crosses V_{CHRDY} (selected through the VCHRDY register), if the corresponding event source has been previously enabled through the IRQEN0.VCHRDY field.

- 0: the storage element voltage did not cross V_{CHRDY}.
- 1: the storage element voltage crossed V_{CHRDY}.

Bit [1]: storage element overdischarge (IRQFLG0.VOVDIS)

This IRQ pin event flag is set after $T_{CRIT,ST}$ when the storage element voltage drops below V_{OVDIS} (selected through the VOVDIS register) or directly when the storage element rises above V_{OVDIS}, if the corresponding event source has been previously enabled through the IRQEN0.VOVDIS field.

- 0: the storage element voltage did not cross V_{OVDIS}.
- 1: the storage element voltage crossed V_{OVDIS}.

Bit [0]: I2C interface ready (IRQFLG0.I2CRDY)

This IRQ pin event flag is set when the serial interface (I^2C) is ready to communicate, if the corresponding event source has been previously enabled through the IRQEN0.I2CRDY field.

- 0: I^2C interface not yet ready to communicate.
- 1: I^2C interface became ready to communicate.

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9.10.2. IRQFLG1

The IRQFLG1 register is the IRQ pin event flags register 1.

IRQFLG1 register		Address: 0x14		Access: R		Reset: 0x00
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1:0]
CHG5VON	CHG5VCONN	APMERR	APMDONE	TEMPDONE	STODONE	RESERVED
0x00	0x00	0x00	0x00	0x00	0x00	-

Table 45: IRQFLG1 register

Bit [7]: 5 V charger charging (IRQFLG1.CHG5VON)

This IRQ pin event flag is set when the 5 V charger starts or stops to charge the storage element, if the corresponding event source has been previously enabled through the IRQEN1.CHG5VON field.

- 0: the 5 V charger has not started or stopped to charge.
- 1: the 5 V charger has started or stopped to charge.

Bit [6]: 5 V charger connected (IRQFLG1.CHG5VCONN)

This IRQ pin event flag is set when the 5 V charger gets connected or disconnected (see Table 6 for V_{5V_IN} requirements), if the corresponding event source has been previously enabled through the IRQEN1.CHG5VCONN field.

- 0: the 5 V charger has not been connected or disconnected.
- 1: the 5 V charger has been connected or disconnected.

Bit [5]: APM error (IRQFLG1.APMERR)

This IRQ pin event flag is set when an APM error occurs, if the corresponding event source has been previously enabled through the IRQEN1.APMERR field.

- 0: no APM error occurred.
- 1: an APM error occurred.

When an APM error occurs, the APMERR register is used along with the IRQFLG1.APMERR field, see Section 9.14.

Bit [4]: APM done (IRQFLG1.APMDONE)

This IRQ pin event flag is set when new APM data is available, if the corresponding event source has been previously enabled through the IRQEN1.APMDONE field.

- 0: no new APM data available.
- 1: new APM data available.

Bit [3]: temperature measurement done (IRQFLG1.TEMPDONE)

This IRQ pin event flag is set when the temperature measurement is done, if the corresponding event source has been previously enabled through the IRQEN1.TEMPDONE field.

- 0: temperature measurement not completed.
- 1: temperature measurement completed.

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Bit [2]: storage element voltage measurement done (IRQFLG1.STODONE)

This IRQ pin event flag is set when the storage element voltage measurement is done, if the corresponding event source has been previously enabled through the IRQEN1.STODONE field.

- 0: storage element voltage measurement not completed.
- 1: storage element voltage measurement completed.

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9.11. Status (STATUSx)

9.11.1. STATUS0

The STATUS0 register provides information about the SPM10140's status (along with the STATUS1 register).

STATUS0 register	Address: 0x15		Access: R		Reset: 0x00	
Bit [7:6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	CHG5VON	CHG5VCONN	RESERVED	OVCH	CHRDY	OVDIS
-	0x00	0x00	-	0x00	0x00	0x00

Table 46: STATUS0 register

Bit [5]: 5 V charger charging (STATUS0.CHG5VON)

This status indicates whether the 5 V charger is actively charging the storage element or not.

- 0: the 5 V charger is not charging.
- 1: the 5 V charger is charging.

Bit [4]: 5 V charger connected (STATUS0.CHG5VCONN)

This status indicates whether the 5 V charger is considered connected or not (see Table 6 for V_{5V_IN} requirements).

- 0: the 5 V charger is disconnected.
- 1: the 5 V charger is connected.

Bit [2]: storage element overcharge (STATUS0.OVCH)

This status indicates whether the storage element voltage is higher than V_{OVCH} or not.

- 0: the storage element voltage is lower than the overcharge threshold.
- 1: the storage element voltage is equal or higher than the overcharge threshold.

Bit [1]: storage element charge-ready (STATUS0.CHRDY)

This status indicates whether the storage element voltage is higher than V_{CHRDY} or not.

- 0: the storage element voltage is lower than the charge-ready threshold.
- 1: the storage element voltage is equal or higher than the charge-ready threshold.

Bit [0]: storage element overdischarge (STATUS0.OVDIS)

This status indicates whether the storage element voltage has been lower than V_{OVDIS} for more than $T_{CRIT,ST}$ or not.

- 0: the storage element voltage has not been equal or lower than the overdischarge threshold for more than $T_{CRIT,ST}$.
- 1: the storage element voltage has been equal or lower than the overdischarge threshold for more than $T_{CRIT,ST}$.

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9.11.2. STATUS1

The STATUS1 register provides information about the SPM10140's status (along with the STATUS0 register).

STATUS1 register	Address: 0x16	Access: R		Reset: 0x00
Bit [7:4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	TEMPHOTDIS	TEMPCOLDDIS	TEMPHOTCH	TEMPCOLDCH
-	0x00	0x00	0x00	0x00

Table 47: STATUS1 register

Bit [3]: storage element discharge maximum temperature (STATUS1.TEMPHOTDIS)

This status indicates whether the temperature is higher than the hot threshold (for storage element discharging) or not.

- 0: the temperature is below the hot threshold.
- 1: the temperature is equal or above the hot threshold.

Bit [2]: storage element discharge minimum temperature (STATUS1.TEMPCOLDDIS)

This status indicates whether the temperature is lower than the cold threshold (for storage element discharging) or not.

- 0: the temperature is above the cold threshold.
- 1: the temperature is equal or below the cold threshold.

Bit [1]: storage element charge maximum temperature (STATUS1.TEMPHOTCH)

This status indicates whether the temperature is higher than the hot threshold (for storage element charging) or not.

- 0: the temperature is below the hot threshold.
- 1: the temperature is equal or above the hot threshold.

Bit [0]: storage element charge minimum temperature (STATUS1.TEMPCOLDCH)

This status indicates whether the temperature is lower than the cold threshold (for storage element charging) or not.

- 0: the temperature is above the cold threshold.
- 1: the temperature is equal or below the cold threshold.

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9.12. APM Data Summary (APMxLOAD)

The values in the APM data registers can be computed by left bit-shifting by the value in the OFFSET field to obtain the measured APM power (P_{APM}) and energy (E_{APM}) provided from the storage element to the LOAD output during the previous APM window (see Section 5.5):

$$P_{APM} = (\text{POWER} \ll \text{OFFSET}) \times \alpha$$

$$E_{APM} = P_{APM} \times \text{APM window}$$

Where:

P_{APM} is the average power (W) provided from the storage element during the previous APM window.

α is the correction factor used to convert the APM values from the APMxLOAD registers into power. This alpha factor takes into account the variability between devices, the board layout, and the effective value of L_{BUCK}, as well as several other parameters that affect the APM conversion. The alpha factor can be determined by calibrating the complete system to take all these parameters into account. Please contact e-peas support for more details about alpha calibration.

E_{APM} is the energy (J) provided from the storage element during the previous APM window.

APM window is the duration (s) used to calculate E_{APM}. It must match the actual APM window duration, which may slightly deviate from the nominal datasheet value $T_{APM,WINDOW}$ (see Table 7).

	APM2LOAD								APM1LOAD								APM0LOAD							
	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Register fields	APM2LOAD.DATA[7:0]								APM1LOAD.DATA[7:0]								APM0LOAD.DATA[7:0]							
Global APM Field	APM DATA [23:0]																							
Power Meter Fields	OFFSET [4:0]					POWER [18:16]			POWER [15:8]								POWER [7:0]							

Table 48: Summary of APMxLOAD register fields

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9.13. LOAD APM Data (APMxLOAD)

9.13.1. APM0LOAD

The APM0LOAD is the first register providing the LOAD APM data.

APM0LOAD register	Address: 0x1A	Access: R	Reset: 0x00
Bit [7:0]			
DATA			
0x00			

Table 49: APM0LOAD register

Bit [7:0]: LOAD APM data (APM0LOAD.DATA)

This register contains the bits [7:0] of the LOAD APM data. See Section 9.12 for APM formulas based on register value.

9.13.2. APM1LOAD

The APM1LOAD is the second register providing the LOAD APM data.

APM1LOAD register	Address: 0x1B	Access: R	Reset: 0x00
Bit [7:0]			
DATA			
0x00			

Table 50: APM1LOAD register

Bit [7:0]: LOAD APM data (APM1LOAD.DATA)

This register contains the bits [15:8] of the LOAD APM data. See Section 9.12 for APM formulas based on register value.

9.13.3. APM2LOAD

The APM2LOAD is the third register providing the LOAD APM data.

APM2LOAD register	Address: 0x1C	Access: R	Reset: 0x00
Bit [7:0]			
DATA			
0x00			

Table 51: APM2LOAD register

Bit [7:0]: LOAD APM data (APM2LOAD.DATA)

This register contains the bits [23:16] of the LOAD APM data. See Section 9.12 for APM formulas based on register value.

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9.14. APM Error (APMERR)

The APMERR register provides the APM errors status.

APMERR register	Address: 0x1D	Access: R	Reset: 0x00
Bit [7:2]		Bit [1]	Bit [0]
RESERVED		LOADERR	RESERVED
-		0x00	-

Table 52: APMERR register

Bit [1]: LOAD APM data error (APMERR.LOADERR)

This field indicates whether the LOAD APM data is corrupted or not, which occurs when V_{LOAD} > (V_{STO} - 0.25 V). In this case, the buck converter runs in “bang-bang” controlled converter mode (see Section 5.2).

- 0: the LOAD APM data is valid.
- 1: the LOAD APM data is corrupted.

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9.15. Temperature Monitoring Data (TEMP)

The TEMP register allows providing the temperature monitoring data as long as R_{DIV} and R_{TH} are connected (see Figure 10).

TEMP register	Address: 0x1E	Access: R	Reset: 0x00
Bit [7:0]			
DATA			
0x00			

Table 53: TEMP register

Bit [7:0]: temperature monitoring data (TEMP.DATA)

This field gives the code that results from the temperature monitoring.

R_{TH} can be determined using the following equation:

$$R_{TH} = \frac{R_{DIV} \times DATA}{256 - DATA}$$

Thus the temperature T in Kelvin can be obtained with the following formula.

$$T = \frac{B}{\ln\left(\frac{R_{TH}}{R0}\right) + \frac{B}{T_0}}$$

See Section 5.4 for further information.

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9.16. Storage Element Voltage Data (STO)

The STO register allows providing the storage element monitoring data.

STO register	Address: 0x1F	Access: R	Reset: 0x00
Bit [7:0]			
DATA			
0x00			

Table 54: STO register

Bit [7:0]: storage element monitoring data (STO.DATA)

This field contains the code that results from the storage element monitoring.

V_{STO} can be determined using the following formula:

$$V_{STO} = \frac{4.8 \times DATA}{256}$$

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10. Typical Application Circuits

10.1. Example Circuit 1

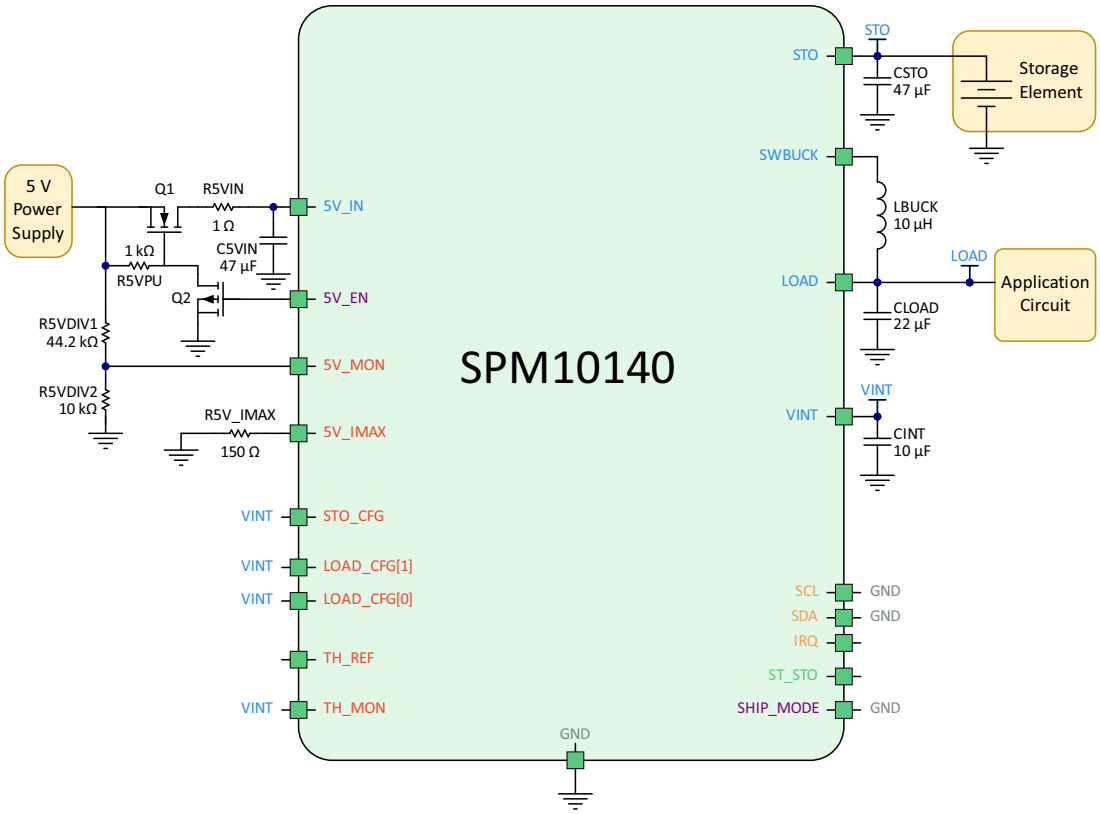


Figure 14: Typical application circuit 1

Figure 14 shows a typical application circuit of the SPM10140.

- The application circuit must be supplied with 3.30 V:
  - LOAD_CFG[1:0] = HH
    - V_{LOAD} = 3.30 V
- The storage element is a Lithium-ion battery. The protection thresholds are configured as follows:
  - STO_CFG = H
    - V_{OVDIS} = 3.00 V
    - $V_{OVDIS,BUCK}$ = V_{LOAD}
    - V_{CHRDY} = 3.20 V
    - $V_{CHRDY,BUCK}$ = 3.50 V
    - V_{OVCH} = 4.15 V
    - $V_{OVCH,LOW}$ = V_{OVCH} - V_{HYST} = 4.11 V
- The 5 V charger is used with the overvoltage protection circuit and a charging current of 400 mA (R_{5V_IMAX} = 150 Ω).

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- The temperature monitoring is not used:
  - TH_MON is connected to VINT.
  - TH_REF is left floating.
- The shipping mode is not used:
  - SHIP_MODE is connected to GND.
- The I²C interface is not used:
  - SCL and SDA are connected to GND.
  - IRQ is left floating.

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10.2. Example Circuit 2

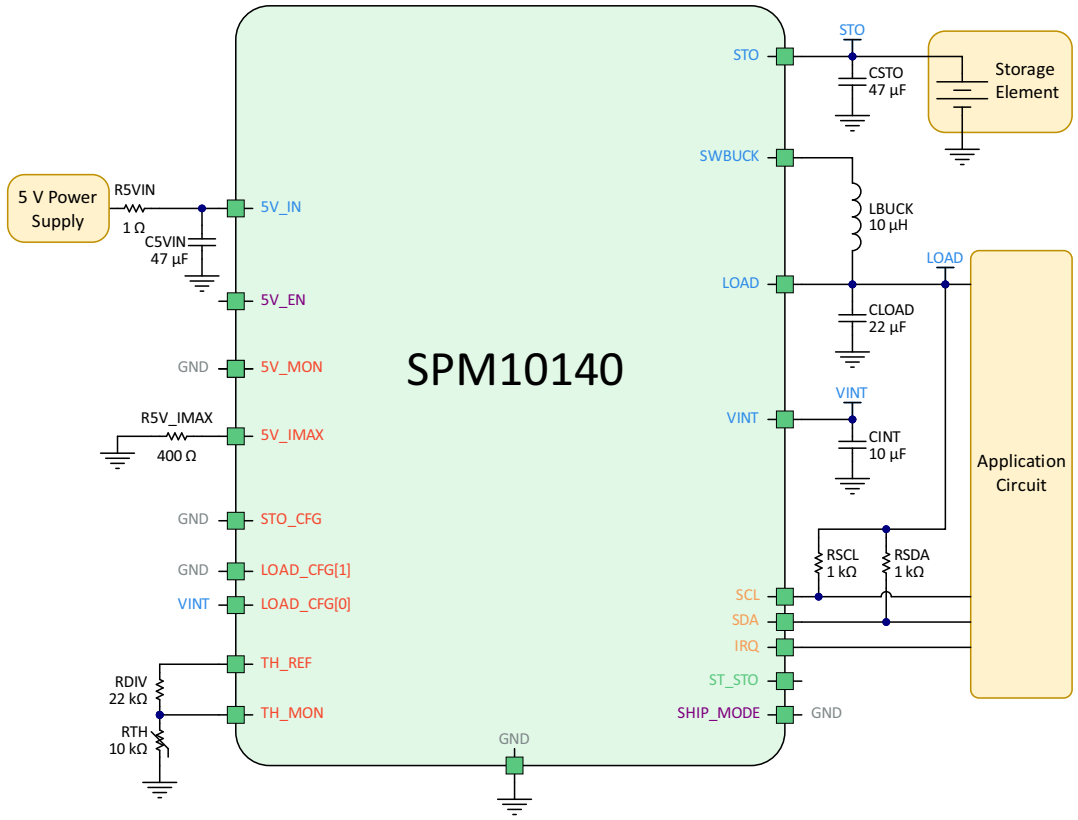


Figure 15: Typical application circuit 2

Figure 15 shows a typical application circuit of the SPM10140.

- The storage element is a Lithium-ion Capacitor (LiC).
- The application circuit must be supplied with 2.20 V.
- The 5 V charger is used without overvoltage protection circuit:
  - 5V_MON is connected to GND.
  - 5V_EN is left floating.
  - Only R_{5VIN} and C_{5VIN} are connected with their recommended values (see Table 10) to slow down the rise time of the 5 V power supply.
  - A 400 Ω resistor is used as R_{5V_IMAX} to configure a charging current of 150 mA.
- The temperature monitoring is used to protect the storage element from charging and discharging when temperature is outside the configured range (see Table 55) with the recommended R_{DIV} and R_{TH} (see Table 10).
- The average power monitoring (APM) is used on LOAD with an IRQ flag when new APM data is available (see Table 55).
- The shipping mode is not used:
  - SHIP_MODE is connected to GND.

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To configure the SPM10140 through I²C:

- The I²C bus is supplied with LOAD.
- SCL and SDA are pulled-up to LOAD with 1 kΩ resistors and connected to the application circuit.
- IRQ is connected to the application circuit.
- The I²C registers are configured with the configurations described in Table 55. The unmodified registers will be configured with their reset values (see Table 18).

Address	Register name	Value	Description
0x02	VOVDIS	0x04	V_{OVDIS} = 2.50 V
0x03	VCHRDY	0x04	V_{CHRDY} = 2.60 V
0x04	VOVCH	0x16	V_{OVCH} = 3.80 V
0x07	BUCKCFG	0x01	Buck converter output enable V_{LOAD} = 2.20 V
0x08	VCHRDYBUCK	0x04	$V_{CHRDY,BUCK}$ = 2.60 V
0x0A	TEMPCOLDCH	0xC6	Minimum -20°C for charge.
0x0B	TEMPHOTCH	0x1B	Maximum +65°C for charge.
0x0C	TEMPCOLDDIS	0xC6	Minimum -20°C for discharge.
0x0D	TEMPHOTDIS	0x1B	Maximum +65°C for discharge.
0x0E	TEMPPROTECT	0x0D	Thermal protection enabled. Temperature hysteresis = 6 ADC steps (23.4 mV).
0x0F	APM	0x02	LOAD APM enabled.
0x10	IRQEN0	0x61	I2CRDY IRQ flag enabled. TEMPCH IRQ flag enabled. TEMPDIS IRQ flag enabled.
0x11	IRQEN1	0x18	TEMPDONE IRQ flag enabled. APMDONE IRQ flag enabled.
0x12	CTRL	0x01	Write this register after writing the others to load the I²C new register configuration.

Table 55: Typical application circuit 2 I²C configurations

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11. Circuit Behavior

11.1. Startup from 5V_IN

11.1.1. Configuration

- The 5 V charger is used without the overvoltage protection circuit:
  - 5 V voltage source connected to 5V_IN through R_{5VIN} and C_{5VIN}
  - 5V_EN is left floating and 5V_MON connected to GND
- R_{5V_IMAX} = 445 Ω
  - $I_{5V,CC}$ = 135 mA
- STO: 5 F supercapacitor charged at 2.80 V beforehand
- STO_CFG = H:
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.20 V
  - V_{OVCH} = 4.15 V
  - $V_{OVDIS,BUCK}$ = V_{LOAD}
  - $V_{CHRDY,BUCK}$ = 3.50 V
- LOAD_CFG[1:0] = HH:
  - V_{LOAD} = 3.30 V
- L_{BUCK} = 10 µH
- The thermal monitoring is not used:
  - TH_MON is connected to VINT
  - TH_REF is left floating
- The I²C communication is used:
  - The I2CRDY IRQ is the only enabled IRQ flag
- SHIP_MODE = L:
  - Shipping mode is disabled

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11.1.2. Observations

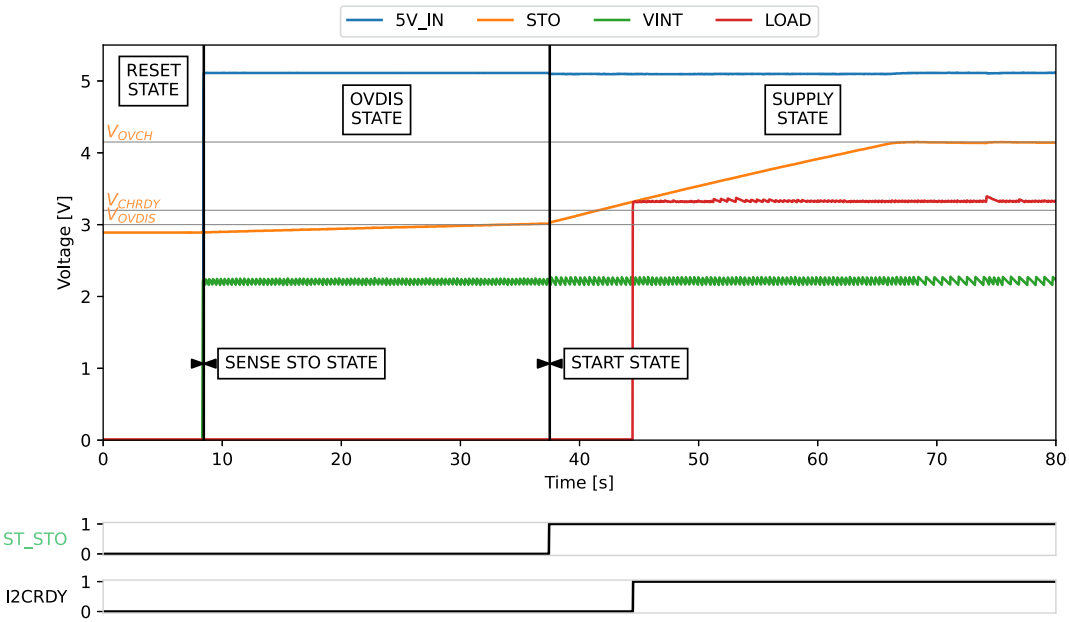


Figure 16: Startup from 5V_IN behavior

- The SPM10140 is initially in RESET STATE.
- Once the supply connected on 5V_IN is switched on, the SPM10140 coldstarts. C_{INT} is charging until VINT reaches $V_{INT,CS}$. The SPM10140 switches then to SENSE STO STATE.
- In SENSE STO STATE, the SPM10140 measures V_{STO}, which is below V_{OVDIS}. It switches then directly to OVDIS STATE.
- In OVDIS STATE, the SPM10140 charges the storage element connected to STO thanks to the 5 V charger with a current equal to $I_{5V,OVDIS,CC}$. VINT is supplied by 5V_IN. Once V_{STO} reaches V_{OVDIS}, the SPM10140 switches to START STATE.
- In START STATE, the 5 V charging current changes to $I_{5V,CC}$. Given that the 5 V charger is charging, the SPM10140 switches directly to SUPPLY STATE without waiting for V_{STO} to reach V_{CHRDY}.
- In SUPPLY STATE, the SPM10140 keeps charging the storage element from 5V_IN with $I_{5V,CC}$. ST_STO pin is asserted.
- Given that the 5 V charger is charging, the LOAD output is enabled when V_{STO} reaches $V_{OVDIS,BUCK}$. V_{LOAD} is then regulated at 3.30 V. Now that V_{LOAD} is available, the I²C bus is supplied. The SPM10140 notifies the application MCU when the I²C communication is ready thanks to the I2CRDY flag through the IRQ pin. In this example, the IRQFLG0 register is not read by the application. The IRQ pin remains HIGH.
- Once V_{STO} reaches V_{OVCH}, the 5 V charger switches to constant voltage (CV) mode. The charging current is reduced progressively. Once $I_{5V,CV}$ drops below $I_{5V,CV,MIN}$, the SPM10140 stops charging the storage element. The charge is resumed when V_{STO} drops below $V_{OVCH,LOW}$.

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11.2. Shutdown

11.2.1. Configuration

- The 5 V charger is used without the overvoltage protection circuit:
  - 5 V voltage source connected to 5V_IN through R_{5VIN} and C_{5VIN}
  - 5V_EN is left floating and 5V_MON connected to GND
- R_{5V_IMAX} = 1.2 kΩ
  - $I_{5V,CC}$ = 50 mA
- STO: 10 mF electrolytic capacitor charged at 4.00 V beforehand
- STO_CFG = H:
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.20 V
  - V_{OVCH} = 4.15 V
  - $V_{OVDIS,BUCK}$ = V_{LOAD}
  - $V_{CHRDY,BUCK}$ = 3.50 V
- LOAD: 1 kΩ resistor installed between LOAD and GND
- LOAD_CFG[1:0] = HH:
  - V_{LOAD} = 3.30 V
  - I_{LOAD} = 3.30 mA
- L_{BUCK} = 10 µH
- The thermal monitoring is not used:
  - TH_MON is connected to VINT
  - TH_REF is left floating
- The I²C communication is used:
  - The LOADSHTDWN IRQ is the only enabled IRQ flag
- SHIP_MODE = L:
  - Shipping mode is disabled

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11.2.2. Observations

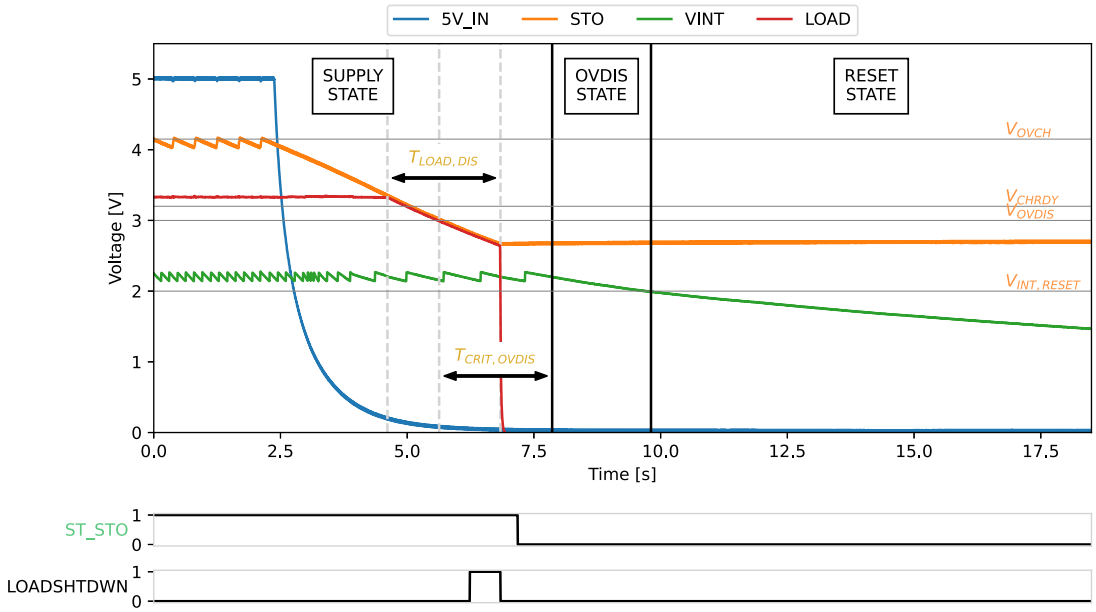


Figure 17: Shutdown behavior

- The SPM10140 is initially in SUPPLY STATE. ST_STO is HIGH and VINT is supplied by STO. The power provided by the 5V_IN input is higher than the one drained by the LOAD output, so the storage element voltage is maintained around V_{OVCH}.
- Around 2.5 s, the 5 V power supply is disconnected from 5V_IN. The storage element is not charging anymore. Its voltage decrease gradually as the LOAD output power is drained.
- When V_{STO} drops below $V_{OVDIS,BUCK}$, which is equal to V_{LOAD}, the SPM10140 waits for $T_{CRIT,LOAD}$ to rise the LOADSHTDWN IRQ flag, and for $T_{LOAD,DIS}$ to disable the LOAD output. During $T_{LOAD,DIS}$, V_{LOAD} is equal to V_{STO}. This is not due to the bypass feature as it is disabled, but to the fact that V_{STO} is below the LOAD regulation target.
- After this point, the storage element is no longer discharging through the LOAD output.
- When V_{STO} drops below V_{OVDIS}, the SPM10140 waits for $T_{CRIT,ST}$ to set ST_STO LOW, and for $T_{CRIT,OVDIS}$ to switch to OVDIS STATE.
- In OVDIS STATE, VINT can only be supplied by the 5V_IN input. Given that the 5 V power supply has previously been disconnected, VINT is not supplied anymore.
- When V_{INT} drops below $V_{INT,RESET}$, the SPM10140 switches to RESET STATE.
- In RESET STATE, the energy present on the storage element is preserved as the STO pin is set to high impedance.

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11.3. Shipping Mode Ignore

11.3.1. Configuration

- The 5 V charger is not used:
  - 5V_IN, 5V_IMAX and 5V_EN are left floating
  - 5V_MON is connected to GND
- STO: 10 mF electrolytic capacitor charged at 3.10 V beforehand
- STO_CFG = H:
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.20 V
  - V_{OVCH} = 4.15 V
  - $V_{OVDIS,BUCK}$ = V_{OVDIS}
  - $V_{CHRDY,BUCK}$ = 3.20 V
- LOAD: application circuit connected
- LOAD_CFG[1:0] = LH:
  - V_{LOAD} = 2.20 V
  - I_{LOAD} = 50 µA
- L_{BUCK} = 10 µH
- The thermal monitoring is not used:
  - TH_MON is connected to VINT
  - TH_REF is left floating
- The I²C communication is not used:
  - SCL and SDA are connected to GND
  - IRQ is left floating
- SHIP_MODE: used to coldstart the SPM10140 (see Figure 18 and Figure 19)

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11.3.2. Observations

When using the SPM10140 SHIP_MODE pin to coldstart, if **the application circuit acts to stay out of the shipping mode**, the system behaves as follows:

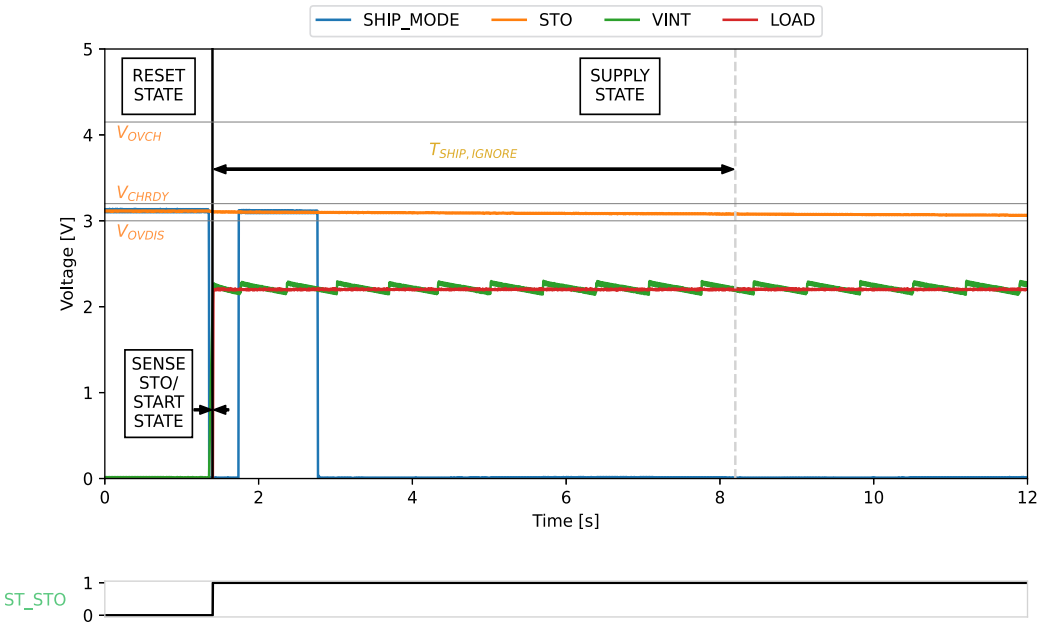


Figure 18: SHIP_MODE ignore behavior with application circuit action

- The SPM10140 is initially in RESET STATE. The SHIP_MODE pin is HIGH to keep the SPM10140 in shipping mode.
- Around 1.5 s, the SHIP_MODE pin is manually forced LOW by the user to trigger the SPM10140 cold start from STO.
- When detecting SHIP_MODE LOW, the SPM10140 goes through the SENSE STO STATE, START STATE and switches directly to SUPPLY STATE given that the storage element voltage (V_{STO}) is already above V_{OVDIS} and $V_{OVDIS,BUCK}$.
- From this point, ST_STO pin is asserted, $T_{SHIP,IGNORE}$ is started, and the LOAD output is enabled and regulated to the configured V_{LOAD}. The application circuit is now supplied.
- Around 1.8 s, the SHIP_MODE pin is released by the user, thus rising back to its HIGH level (V_{STO}). The SPM10140 remains out of the shipping mode as long as $T_{SHIP,IGNORE}$ has not elapsed even if SHIP_MODE is back HIGH.
- Around 2.8 s, the application circuit pulls and maintains the SPM10140 SHIP_MODE pin LOW.
- At the end of $T_{SHIP,IGNORE}$, the SPM10140 resumes the monitoring of SHIP_MODE pin state. Given that SHIP_MODE pin is maintained LOW, the SPM10140 stays out of shipping mode.

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When using the SPM10140 SHIP_MODE pin to coldstart, if **the application circuit does not act to stay out of the shipping mode**, the system behaves as follows:

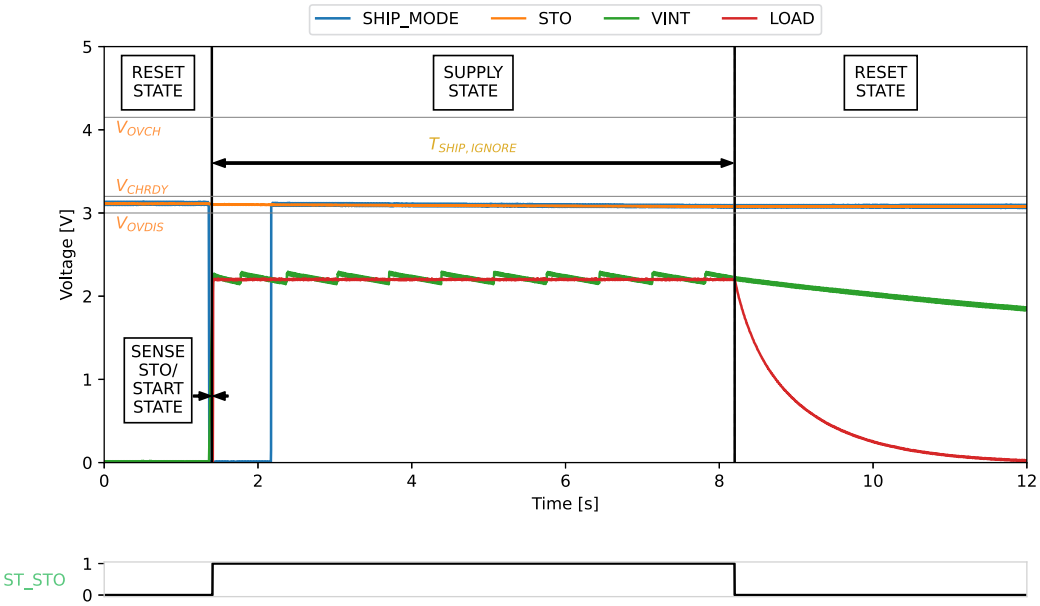


Figure 19: SHIP_MODE ignore behavior without application circuit action

- The SPM10140 is initially in RESET STATE. The SHIP_MODE pin is HIGH to keep the SPM10140 in shipping mode.
- Around 1.3 s, the SHIP_MODE pin is manually forced LOW by the user to trigger the SPM10140 cold start from STO.
- When detecting SHIP_MODE LOW, the SPM10140 goes through the SENSE STO STATE, START STATE and switches directly to SUPPLY STATE given that the storage element voltage (V_{STO}) is already above V_{OVDIS} and $V_{OVDIS,BUCK}$.
- From this point, ST_STO pin is asserted, $T_{SHIP,IGNORE}$ is started, and the LOAD output is enabled and regulated to the configured V_{LOAD}. The application circuit is now supplied.
- Around 2.1 s, the SHIP_MODE pin is released by the user, thus rising back to its HIGH level (V_{STO}). The SPM10140 remains out of the shipping mode as long as $T_{SHIP,IGNORE}$ has not elapsed even if SHIP_MODE is back HIGH.
- This time, unlike the previous behavior with the application circuit forcing SHIP_MODE pin LOW, the application circuit never pulls the SPM10140 SHIP_MODE pin back LOW.
- At the end of $T_{SHIP,IGNORE}$, the SPM10140 resumes the monitoring of SHIP_MODE pin state. Given that SHIP_MODE pin is back HIGH, the SPM10140 returns in RESET STATE due to the shipping mode. VINT and LOAD are no longer supplied.

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11.4. 5 V Charger Overvoltage Protection

11.4.1. Configuration

- The 5 V charger is used with the overvoltage protection circuit, as explained in Section 5.6.2 (external PSU named 5V_EXT).
- R_{5V_IMAX} = 300 Ω
  - $I_{5V,CC}$ = 200 mA
- STO: 5 F supercapacitor charged at 3.00 V beforehand
- STO_CFG = H:
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.20 V
  - V_{OVCH} = 4.15 V
- LOAD_CFG[1:0] = LL:
  - The LOAD output is disabled
- The thermal monitoring is not used:
  - TH_MON is connected to VINT
  - TH_REF is left floating
- The I²C communication is not used:
  - SCL and SDA are connected to GND
  - IRQ is left floating
- SHIP_MODE = L:
  - Shipping mode is disabled

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11.4.2. Observations

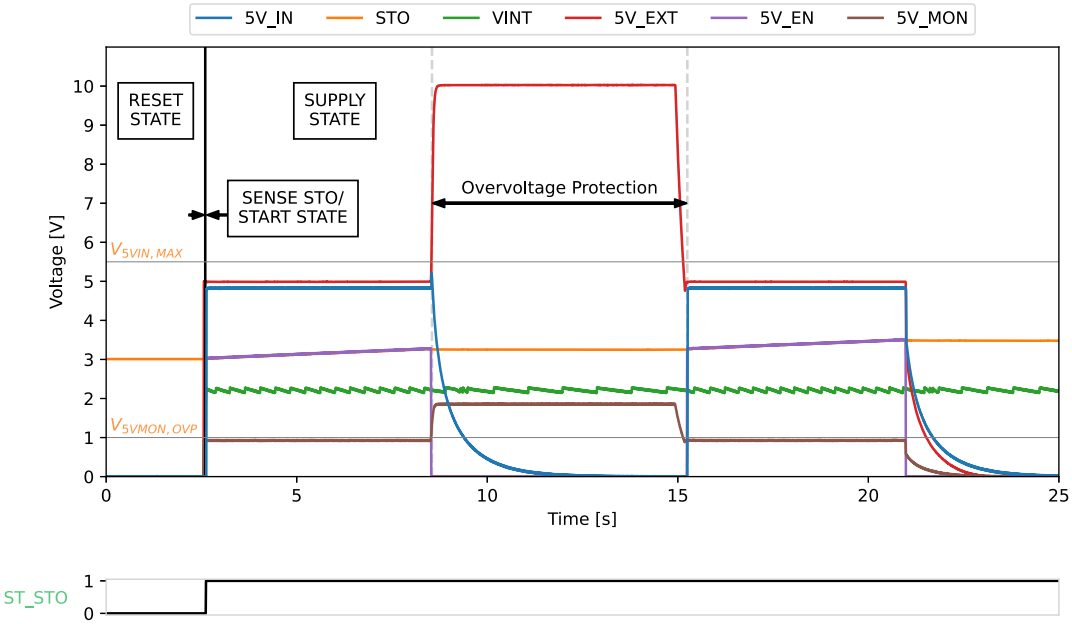


Figure 20: 5 V charger overvoltage protection behavior

- The SPM10140 is initially in RESET STATE.
- When the 5V_EXT supply connected on the 5 V charger protection circuit input is switched on, the SPM10140 detects through the 5V_MON pin that a suitable power supply is connected. The SPM10140 coldstarts from the storage element connected to STO.
- When V_{INT} reaches $V_{INT,CS}$, the SPM10140 goes through the SENSE STO STATE and START STATE. The power path between the 5V_EXT power supply and 5V_IN is enabled thanks to the 5V_EN pin, as explained in Section 5.6.2.
- Given that the storage element voltage (V_{STO}) is already above V_{OVDIS} and the 5 V charger is charging, the SPM10140 switches directly to SUPPLY STATE.
- In SUPPLY STATE, ST_STO is asserted and the SPM10140 charges the storage element connected to STO thanks to its 5 V charger. The 5V_EXT power supply voltage is continuously monitored through 5V_MON.
- Around 8.5 s, the voltage on the 5V_EXT power supply rises up to 10 V, which is higher than the maximum sustainable 5V_IN voltage. The SPM10140 directly detects this overvoltage due to 5V_MON voltage rising above $V_{5V_MON,OVP}$. The overvoltage protection circuit is triggered through 5V_EN to protect the SPM10140. VINT remain supplied by STO.
- Around 15.1 s, the 5V_EXT power supply voltage drops back to 5 V, meaning that 5V_MON voltage is back below $V_{5V_MON,OVP}$. The SPM10140 sets 5V_EN HIGH to resume the storage element charge with the 5 V charger.
- Around 21 s, the 5V_EXT power supply is disconnected. VINT remain supplied by STO.

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11.5. Buck Converter Bypass Mode

11.5.1. Configuration

- The 5 V charger is used without the overvoltage protection circuit:
  - 5 V voltage source connected to 5V_IN through R_{5VIN} and C_{5VIN}
  - 5V_EN is left floating and 5V_MON connected to GND
- R_{5V_IMAX} = 1.2 kΩ
  - $I_{5V,CC}$ = 50 mA
- STO: 20 mF electrolytic capacitor
  - V_{OVDIS} = 2.80 V
  - V_{CHRDY} = 3.20 V
  - V_{OVCH} = 4.15 V
  - $V_{OVDIS,BUCK}$ = V_{LOAD}
  - $V_{CHRDY,BUCK}$ = 3.50 V
- LOAD: 6.8 kΩ resistor installed between LOAD and GND
- LOAD_CFG[1:0] = HH:
  - V_{LOAD} = 3.30 V
  - I_{LOAD} = 220 µA
- L_{BUCK} = 10 µH
- The thermal monitoring is not used:
  - TH_MON is connected to VINT
  - TH_REF is left floating
- The I²C communication is used to configure the storage element thresholds and BUCKCFG.BYPASSEN field
- SHIP_MODE = L:
  - Shipping mode is disabled

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11.5.2. Observations

When using the SPM10140 LOAD output **without bypass mode**, the system behaves as follows:

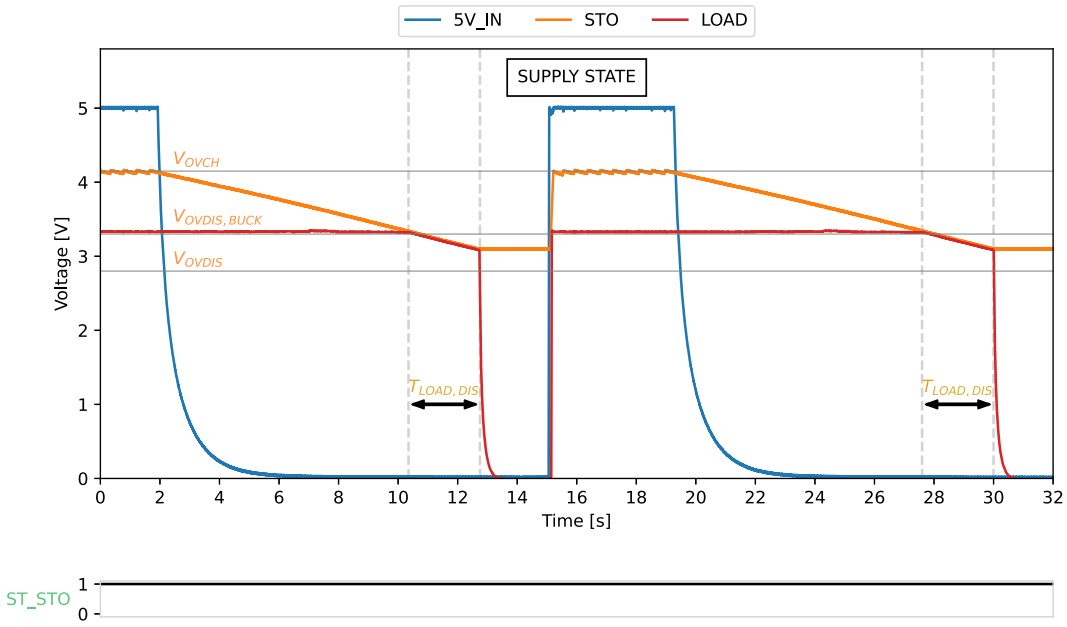


Figure 21: LOAD behavior without bypass mode

- The SPM10140 is initially in SUPPLY STATE with ST_STO HIGH. The 5 V charger is connected and maintains V_{STO} regulated around V_{OVCH}. The LOAD output is enabled and regulated to the configured V_{LOAD}.
- Around 2 s, the 5 V charger is disconnected. V_{STO} is no longer maintained to V_{OVCH}. The storage element is discharging due to the LOAD output current.
- Given that the buck converter bypass mode is disabled, when V_{STO} drops below $V_{OVDIS,BUCK}$, which is equal to V_{LOAD}, $T_{LOAD,DIS}$ timer is started. During $T_{LOAD,DIS}$, V_{LOAD} is equal to V_{STO}. This is not due to the bypass feature as it is disabled, but to the fact that V_{STO} is below the LOAD regulation target.
- When $T_{LOAD,DIS}$ elapses, the LOAD output is disabled. The storage element is no longer discharging through the LOAD. The SPM10140 remains in SUPPLY STATE as V_{STO} remains above V_{OVDIS}.
- Around 15 s, the 5 V charger is connected back and used to charge the storage element. As soon as V_{STO} reaches $V_{OVDIS,BUCK}$, the LOAD output is enabled again.

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When using the SPM10140 LOAD output **with bypass mode**, the system behaves as follows:

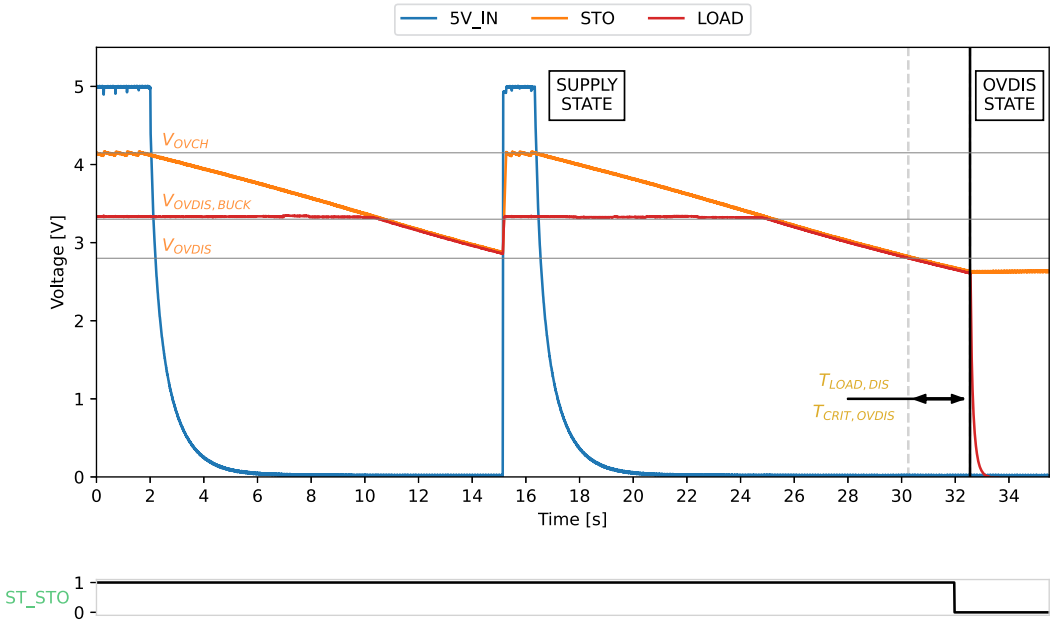


Figure 22: LOAD behavior with bypass mode

- The SPM10140 is initially in SUPPLY STATE with ST_STO HIGH. The 5 V charger is connected and maintains V_{STO} regulated around V_{OVCH}. The LOAD output is enabled and regulated to the configured V_{LOAD}.
- Around 2 s, the 5 V charger is disconnected. V_{STO} is no longer maintained to V_{OVCH}. The storage element is discharging due to the LOAD output current.
- Given that the buck converter bypass mode is enabled, when V_{STO} drops below $V_{OVDIS,BUCK}$ for more than $T_{LOAD,DIS}$, the SPM10140 does not disable its LOAD output. LOAD is shorted to STO as long as the SPM10140 remains in SUPPLY STATE and V_{STO} remains below $V_{OVDIS,BUCK}$.
- Around 15 s, the 5 V charger is connected back and used to charge the storage element for a few seconds, making V_{STO} rise above $V_{OVDIS,BUCK}$, thus, enabling back the LOAD output.
- Around 30.2 s, V_{STO} drops below V_{OVDIS}. At this moment, $T_{LOAD,DIS}$ and $T_{CRIT,OVDIS}$ are started.
- When the timers elapse, the LOAD output is disabled and the SPM10140 switches to OVDIS STATE.

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12. Minimum BOM

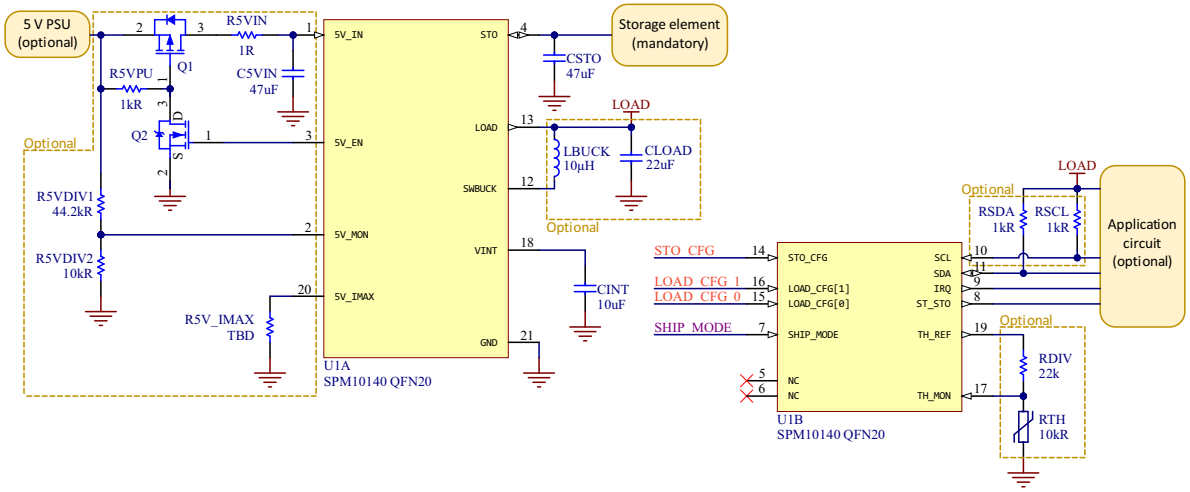


Figure 23: Schematic

Designator		Description	Qty	Manufact.	Part Number
Mandatory	U1	SPM10140	1	e-peas	order at sales@e-peas.com
	Storage Element	Min. voltage 1.50 V Max. voltage 5.00 V	1	To be defined by the user.	
	CINT	Ceramic capacitor 10 µF, 6.3 V, 20 %, X5R, 0402	1	Murata	GRM155R60J106ME
	CSTO[1]	Ceramic capacitor 47 µF 6.3 V 20 % X5R, 0603	1	Murata	GRM188R60J476ME
Optional	LBUCK	Power inductor 10 µH	1	TDK	VLS252012CX-100M-1
	CLOAD	Ceramic capacitor 22 µF, 10 V, 20 %, X5R, 0603	1	Murata	GRM188R61A226ME
	R5V_IMAX	Resistor	1	To be defined by the user.	
	C5VIN	Ceramic capacitor 47 µF 6.3 V 20 % X5R, 0603	1	Murata	GRM188R60J476ME
	R5VIN	Resistor 1 Ω	1	Vishay	CRCW08051R00FK
	Q1	Power MOSFET, P channel	1	Diodes Inc.	DMG2305UX
	Q2	Power MOSFET, N channel	1	Diodes Inc.	BSS138-7-F
	R5VPU	Resistor 1 kΩ	1	Multicomp	MCWR06X1001FTL
	R5VDIV1	Resistor 44.2 kΩ	1	Yageo	RC0402FR-0744K2L
	R5VDIV2	Resistor 10 kΩ	1	Yageo	RC0402FR-0710KL
	RSCL	Resistor 1 kΩ	1	Multicomp	MCWR06X1001FTL
	RSDA	Resistor 1 kΩ	1	Multicomp	MCWR06X1001FTL
	RDIV	Resistor 22 kΩ	1	Yageo	RC0402FR-0722KL
	RTH	10 kΩ NTC thermistor	1	Murata	NCP15XH103J03RC

Table 56: Minimum BOM

1. Recommended CSTO for optimal efficiency, particularly with high-ESR storage elements. If using a smaller value, ensure it meets the minimum requirement (see Table 10).

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13. Layout

13.1. Guidelines

Figure 24 shows an example of PCB layout with SPM10140.

The following guidelines must be applied for best performances:

- Make sure that ground and power signals are routed with large tracks. If an internal ground plane is used, place vias as close as possible to the components, especially for decoupling capacitors.
- Reactive components related to the buck converter must be placed as close as possible to the corresponding pins (SWBUCK, LOAD and STO), and be routed with large tracks/polygons.
- PCB track capacitance must be reduced as much as possible on the buck converter switching node SWBUCK. This is done as follows:
  - Keep the connection between the SWBUCK pin and its corresponding inductor short.
  - Remove the ground and power planes under the SWBUCK node. The polygon on the opposite external layer may also be removed.
  - Increase the distance between SWBUCK and the ground polygon on the external PCB layer where the SPM10140 is mounted.
- When using the SPM10140 5 V charger with higher current configurations (i.e. 200 to 400 mA), careful attention to PCB layout, track width, and thermal management becomes essential:
  - Make sure to use large and short tracks/polygons for 5V_IN and STO nodes.
  - Keep the decoupling capacitors as close as possible to the SPM10140 with large and direct ground returns between the decoupling capacitors ground terminals and the SPM10140 GND pin.
  - Ensure effective thermal management for the SPM10140 by connecting its thermal pad to solid copper planes on the inner and bottom layers using multiple thermal vias.
- PCB track capacitance must be reduced as much as possible on the TH_REF node. Same principle as for SWBUCK may be applied.

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13.2. Example

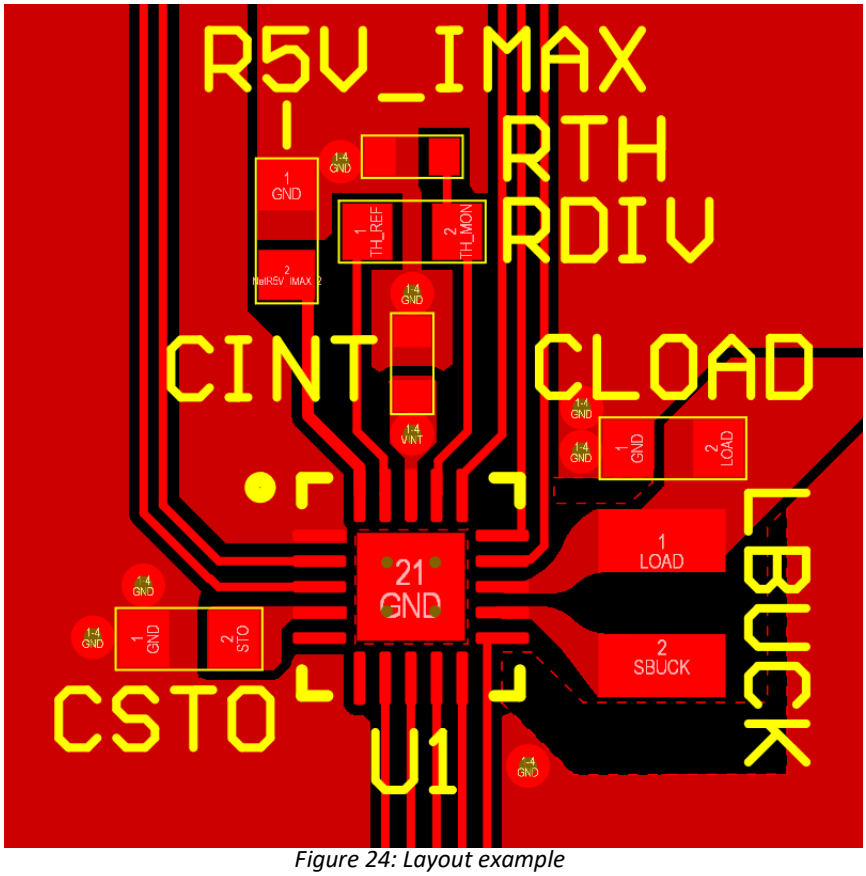


Figure 24: Layout example

13.3. Thermal Considerations

The junction temperature of the device depends directly on the power dissipated within the IC and the thermal characteristics of the PCB assembly.

13.3.1. Power Dissipation Calculation

When operating as a linear regulator, the power dissipated by the SPM10140 is primarily determined by the voltage drop across the IC and the output current.

A first-order estimation of the power dissipation is given by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

For a more accurate estimation, include the quiescent current and internal losses by considering the total input power versus output power:

$$P_D = (V_{IN} \times I_{IN}) - (V_{OUT} \times I_{OUT})$$

Where:

PD = Total power dissipated by the SPM10140 (W)

VIN and IIN = Input voltage (V) and input current (A)

VOUT and IOUT = Output voltage (V) and output current (A)

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13.3.2. Junction Temperature Estimation

The steady-state junction temperature can be estimated using the following relationship:

$$T_J = T_A + (P_D \times \theta JA)$$

Where:

TJ = Junction temperature (°C)

TA = Ambient temperature (°C)

PD = Total power dissipated by the SPM10140 (W), as explained in Section 13.3.1

θJA = Effective junction-to-ambient thermal resistance of the PCB assembly (°C/W)

The effective junction-to-ambient thermal resistance is heavily dependent on the PCB design and application environment. Parameters such as PCB copper area, number of layers, copper thickness, thermal via array, component placement, and local airflow significantly influence overall thermal performance. Consequently, the effective θJA may vary considerably between different applications and PCB implementations.

Users are strongly encouraged to characterize the effective thermal resistance (θJA,eff) of their own PCB assembly under representative operating conditions. This can be achieved by measuring or estimating the junction temperature at thermal equilibrium for a known power dissipation:

$$\theta JA,\text{eff} = \frac{(T_J - T_A)}{P_D}$$

Once characterized, this value can be used to accurately estimate junction temperatures under other operating scenarios within the same application.

13.3.3. Thermal Operating Limits

Thermal performance should always be verified under worst-case operating conditions accounting for:

- Maximum input voltage
- Minimum output voltage
- Maximum output current
- Maximum ambient temperature
- Actual PCB layout and system cooling capabilities
- Worst-case duty cycles or transient modes

The junction temperature must remain below the maximum specified operating limit under all operating conditions (see Table 10). Always maintain an adequate thermal margin to ensure long-term device reliability.

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14. Package Information

14.1. Moisture Sensitivity Level

Package	Parameter	Value
QFN 20-pin 3 x 3 mm	Moisture Sensitivity Level (MSL)[1]	Level 1

Table 57: Moisture sensitivity level

1. According to JEDEC 22-A113 standard.

14.2. RoHS Compliance

e-peas product complies with RoHS requirement.

e-peas defines “RoHS” to mean that semiconductor end-products are compliant with RoHS regulation for all 10 RoHS substances.

This applies to silicon, die attached adhesive, gold wire bonding, lead frames, mold compound, and lead finish (pure tin).

14.3. REACH Compliance

The component and elements used by e-peas subcontractors to manufacture e-peas PMICs and devices are REACH compliant. For more detailed information, please contact e-peas sales team.

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14.4. Package Dimensions

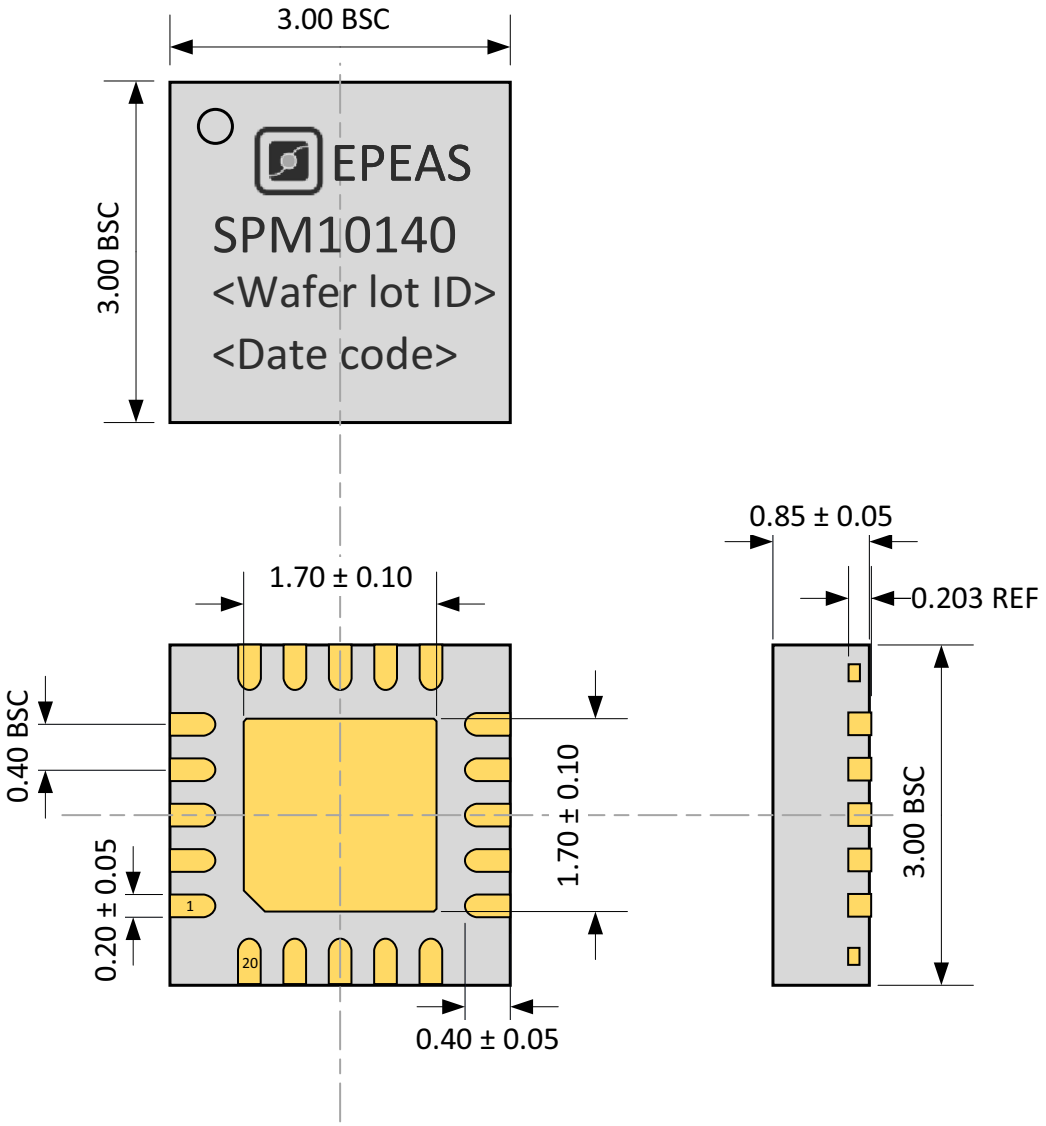


Figure 25: QFN 20-pin 3 x 3 mm drawing (all dimensions in mm)

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14.5. Board Layout

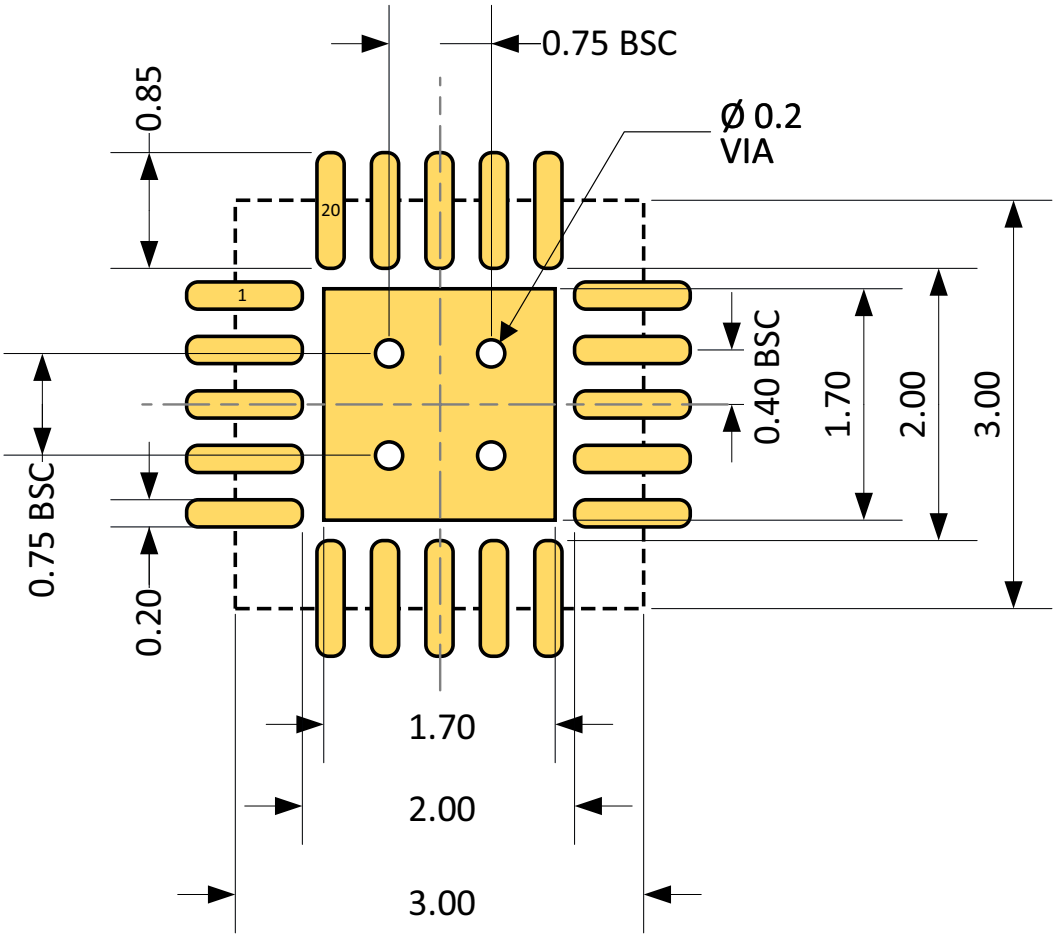


Figure 26: Recommended layout for QFN 20-pin (all dimensions in mm)

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15. Glossary

Symbol	Description
C_{5VIN}	Decoupling capacitor on the 5V_IN pin.
C_{INT}	Decoupling capacitor on the VINT pin.
C_{iss}	Total input capacitance of a MOSFET.
C_{LOAD}	Decoupling capacitor on the LOAD pin.
C_{STO}	Decoupling capacitor on the STO pin.
$I_{5V,CC}$	Current provided to the storage element from the 5 V charger (5V_IN) when in constant current mode and $V_{STO} > V_{OVDIS}$.
$I_{5V,CV,MIN}$	Termination current from which the 5 V charger (5V_IN) stops to charge the storage element in constant voltage mode.
$I_{5V,OVDIS,CC}$	Current provided to the storage element from the 5 V charger (5V_IN) when in constant current mode and $V_{STO} < V_{OVDIS}$.
I_{LOAD}	Current provided from the buck converter output (LOAD).
$I_{LOAD,MAX}$	Maximum current provided from the buck converter output (LOAD).
$I_{Q,RESET}$	SPM10140 internal quiescent current drawn on STO in RESET STATE.
$I_{Q,SHIP}$	SPM10140 internal quiescent current drawn on STO in shipping mode.
$I_{Q,SUPPLY}$	SPM10140 internal quiescent current drawn on STO in SUPPLY STATE.
L_{BUCK}	Buck converter inductor.
Q_1	5 V charger overvoltage protection circuit PMOS.
Q_2	5 V charger overvoltage protection circuit NMOS.
R_{5VDIV1}, R_{5VDIV2}	5 V charger overvoltage protection circuit voltage divider resistors.
R_{5V_IMAX}	Resistor connected between 5V_IMAX and GND that defines the maximum current provided to the storage element by the 5 V charger (5V_IN pin).
R_{5VIN}	Resistor creating a RC filter with C_{5VIN} on 5V_IN pin.
R_{5VPU}	5 V charger overvoltage protection circuit pull-up resistor.
R_{DIV}	Resistor creating with R_{TH} a resistive voltage divider connected to TH_MON. Used for thermal monitoring.
$R_{DS(ON)}$	Drain-to-Source On-Resistance of a MOSFET.
R_{SCL}, R_{SDA}	Pull-up resistors used for the I²C communication bus.
R_{TH}	Thermistor creating with R_{DIV} a resistive voltage divider connected to TH_MON. Used for thermal monitoring.
$T_{5V,MON}$	5V_IN monitoring rate when the 5 V charger is not charging.
$T_{APM,WINDOW}$	Average Power Monitoring (APM) time window.
$T_{CC/CV,TMR}$	5 V charger CC/CV timer duration (see Section 5.6.3).
$T_{CRIT,LOAD}$	Delay triggered when V_{STO} drops below $V_{OVDIS,BUCK}$ or when the temperature exits the discharge temperature range. The SPM10140 sets IRQFLG0.LOADSHTDWN register field HIGH if V_{STO} remains below $V_{OVDIS,BUCK}$ or if the temperature remains outside of the range once $T_{CRIT,LOAD}$ elapses (see Section 5.2)
$T_{CRIT,OVDIS}$	Delay triggered when V_{STO} drops below V_{OVDIS}. The SPM10140 switches to OVDIS STATE once $T_{CRIT,OVDIS}$ elapses (see Section 5.9).
$T_{CRIT,ST}$	Delay triggered when V_{STO} drops below V_{OVDIS}. The SPM10140 sets ST_STO LOW if V_{STO} remains below V_{OVDIS} once $T_{CRIT,ST}$ elapses (see Section 5.9)
$T_{GPIO,MON}$	GPIO monitoring rate.

Table 58: Glossary (part 1)

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Symbol	Description
$T_{LOAD,DIS}$	Delay triggered when V_{STO} drops below $V_{OVDIS,BUCK}$ or when the temperature exits the discharge temperature range. The SPM10140 disables its LOAD output once $T_{LOAD,DIS}$ elapses (see Section 5.2).
$T_{PRE,TMR}$	5 V charger pre-charge timer duration (see Section 5.6.3).
$T_{SHIP,IGNORE}$	Time interval during which the SPM10140 ignores the SHIP_MODE pin state.
$T_{STO,MON}$	Storage element voltage monitoring rate.
$T_{TEMP,MON}$	Thermal monitoring rate.
V_{5V_IN}	Voltage on the 5V_IN pin.
$V_{5V_MON,OVP}$	5V_MON pin voltage above which the 5 V charger overvoltage protection (OVP) circuit is triggered.
V_{CHRDY}	Storage element charge-ready protection threshold (see Section 5.3).
$V_{CHRDY,BUCK}$	Storage element charge-ready buck protection threshold (see Section 5.3).
$V_{GS(TH)}$	Gate-to-Source Threshold Voltage of a MOSFET.
V_{HYST}	Storage element overcharge hysteresis (see Section 5.3).
V_{INT}	Voltage on the VINT pin.
$V_{INT,CS}$	Minimum voltage on VINT for the SPM10140 to switch from RESET STATE to SENSE STO STATE.
$V_{INT,RESET}$	Minimum voltage on VINT before switching to RESET STATE from any other state.
V_{LOAD}	Voltage on the LOAD pin.
V_{OVCH}	Storage element overcharge protection threshold (see Section 5.3).
$V_{OVCH,LOW}$	Storage element overcharge low protection threshold (see Section 5.3).
V_{OVDIS}	Storage element overdischarge protection threshold (see Section 5.3).
$V_{OVDIS,BUCK}$	Storage element overdischarge buck protection threshold (see Section 5.3).
V_{STO}	Voltage on the STO pin.

Table 58: Glossary (part 2)

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16. Revision History

Revision	Date	Description
1.0	November, 2026	Initial release

Table 59: Revision history

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