AEM20941 Evaluation Board User Guide

Description

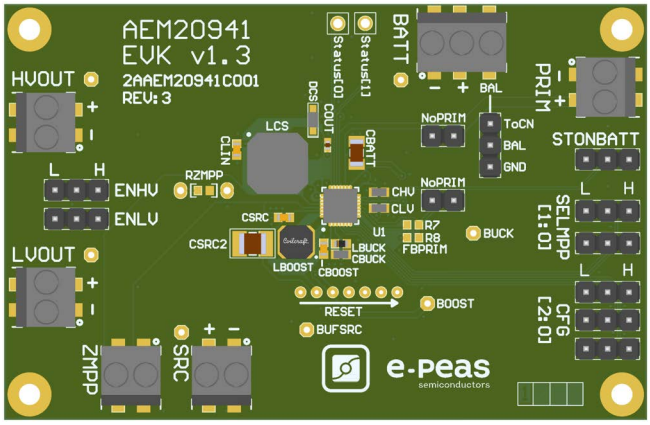
The AEM20941 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM20941 integrated circuit (IC). Please refer to the datasheet for all the useful details about the AEM20941 (Document DS-AEM20941).

The AEM20941 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting.

It allows easy connections to a TEG (Thermo Electric Generator) energy harvester, a storage element, a low-voltage load and a high-voltage load. All the device configurations described in the datasheet can be accessed easily. The control and status signals are available on standard pin headers, allowing users to configure for any usage scenario and evaluate the relevant performance.

The AEM20941 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes…) for the design of a highly efficient subsystem powered by TEG energy harvesting in your target application.

Appearance



Features

Two-way screw terminals

- Source of energy (TEG).
- Low-voltage load.
- High-voltage load.
- Primary battery.
- Resistor for ZMPP configuration.

Three-way screw terminal

- Energy storage element (Battery or (super)capacitor).

3-pin headers

- Maximum power point tracker (MPPT) configuration.
- Low drop-out regulators (LDOs) enabling.
- Energy storage elements and LDOs configuration.
- Dual-cell supercapacitor balancing circuit.
- Start-on-battery configuration.

2-pin headers

- Primary battery configuration.

1-pin headers

- Access to status pins.

Provision for resistors

- Primary battery configuration.
- ZMPP configuration.

Evaluation Kit Information

Part Number	Dimensions
2AAEM20941C001 REV:3	76 mm x 49 mm

Device Information

Part Number	Dimensions
10AEM20941C0001	4 mm x 4 mm

Copyright © 2025 e-peas SA

1. EVK Connection Diagram

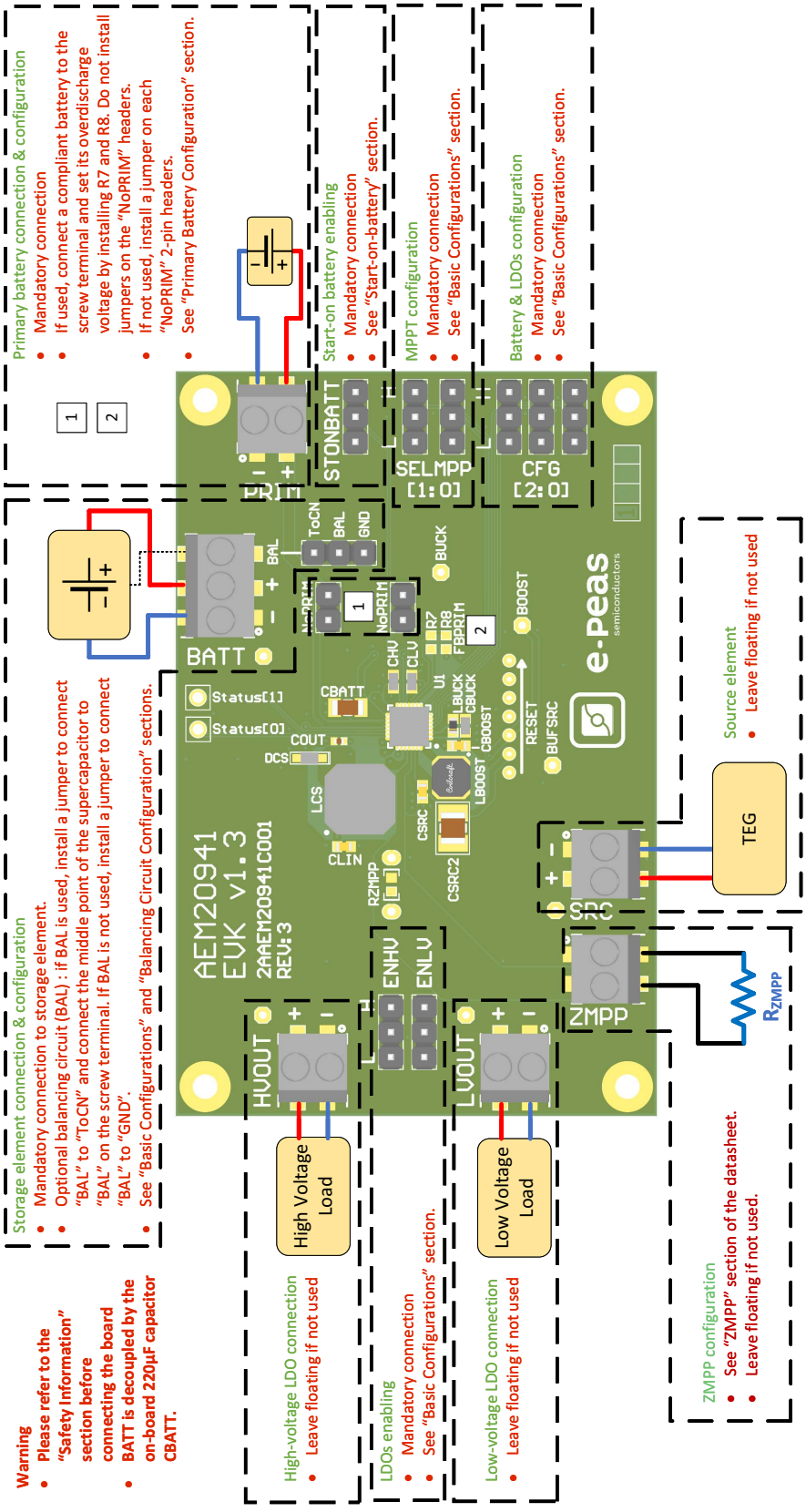


Figure 1: Connection diagram

Copyright © 2025 e-peas SA

2. Pin Configuration and Functions

		If used	If not used
NAME	**FUNCTION**	**CONNECTION**	
Power signals			
SRC	Connection to the harvester.	Connect the source element.	Leave floating.
BATT	Connection to the energy storage element.	Connect the storage element in addition to C_{BATT}[1] (min. 150 µF).	Do not remove C_{BATT}.
BAL	Connection to mid-point of a dual-cell supercapacitor.	Connect mid-point of supercapacitor and a jumper from "BAL" to "ToCN".	Use a jumper to connect "BAL" to "GND".
PRIM	Connection to the primary battery.	Connect primary battery, remove the "NoPRIM" jumpers and install R7/R8 to set the primary battery overdischarge voltage.	Connect a jumper to each "NoPRIM" 2-pin.
LVOUT	Output of the low-voltage LDO regulator.	Connect a load.	Leave floating.
HVOUT	Output of the high-voltage LDO regulator.	Connect a load.	Leave floating.
Debug signals			
BOOST	Output of the boost converter.		
BUCK	Output of the buck converter.		
BUFSRC	Input of the boost converter.		
Configuration signals			
CFG[2:0]	Configuration of the threshold voltages for the energy storage element.	Connect jumpers (see Table 2).	Cannot be left floating.
SELMPP[1:0]	Configuration of the MPP ratio.	Connect jumpers (see Table 4).	Cannot be left floating.
FB_PRIM_D FB_PRIM_U	Configuration of the primary battery.	Use resistors R7-R8 (see Section 3.4.3).	Connect a jumper to each "NoPRIM" 2-pin.
RZMPP	Configuration of the constant impedance ZMPP.	Use resistor RZMPP (see Section 3.4.1).	Leave floating.
STONBATT	Configuration of the start-on-battery feature (see Section 3.4.2).	Connect jumper to "H".	Connect jumper to "L".
Control signals			
ENHV	Enabling pin for the high-voltage LDO (see Table 3).	Connect jumper to "H" if HVOUT LDO is used.	Connect jumper to "L" if HVOUT LDO is not used.
ENLV	Enabling pin for the low-voltage LDO (see Table 3).	Connect jumper to "H" if LVOUT LDO is used.	Connect jumper to "L" if LVOUT LDO is not used.
Status signals			
STATUS[1]	Logic output. Asserted during approximately 600 ms when the storage element voltage falls under V_{OVDIS} or if the AEM20941 is extracting energy from the primary battery. See the "Operating Modes" section from the datasheet for more information.		
STATUS[0]	Logic output. Asserted in NORMAL MODE (when HVOUT/LVOUT are supplied if enabled, see the "Operating Modes" section of the AEM20941 datasheet for more information).		

Table 1: Signals description

1. C_{BATT} capacity on the EVK may vary depending on suppliers availability, with a minimum value of 150 µF (see C_{BATT} value on Figure 15).

Copyright © 2025 e-peas SA

3. General Considerations

3.1. Safety Information

Before using the AEM20941 EVK, always perform these steps in the correct order:

1. Reset the board - see Figure 2.

2. Completely configure the PCB (jumpers/resistors):

- MPP configuration (SELMPP[1:0], R_{ZMPP}) - see Table 4.
- Battery and LDOs configuration (CFG[2:0]) - see Table 2.
- Storage element configuration ("NoPRIM" or R7-R8) - see Section 3.4.3.
- LDOs enabling (ENHV and ENLV) - see Table 3.
- Balancing circuit connection (BAL) - see Section 3.4.4.

3. Connect the storage element on BATT and optionally the primary battery on PRIM.

4. Connect the high and/or low voltage loads on HVOUT/ LVOUT (optional).

5. Connect the harvester on the SRC connector.

Users are urged to follow this procedure to avoid damaging the board.

3.2. AEM20941 Reset

How to reset the AEM20941 evaluation board:

- Disconnect the source.
- Disconnect the storage element.
- Disconnect the optional primary battery.
- Connect the reset pads to GND (from left to right, as indicated on the EVK silkscreen) in order to discharge the internal nodes of the system.

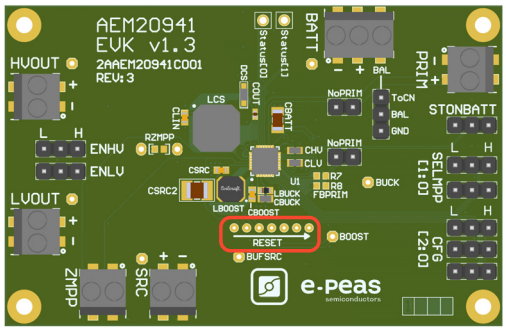


Figure 2: Board reset

Copyright © 2025 e-peas SA

3.3. Basic Configurations

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Reserved for future use.					

Table 2: Usage of CFG[2:0]

Configuration pin	LDO enabling
ENLV	LVOUT
L	Disabled
H	Enabled

Configuration pin	LDO enabling
ENHV	HVOUT
L	Disabled
H	Enabled

Table 3: LDOs enabling

Configuration pins		MPPT ratio
SELMPP[1]	SELMPP[0]	V_{MPP} / V_{OC}
L	L	50%
L	H	55%
H	L	75%
H	H	ZMPPT

Table 4: Usage of SELMPP[1:0]

Copyright © 2025 e-peas SA

3.4. Advanced Configurations

A complete description of the system constraints and configurations is available in the AEM20941 datasheet "System configuration" section.

A reminder on how to calculate the configuration resistors value is provided below. Calculation can be made with the help of the "Configuration Tool" spreadsheet found on e-peas website.

3.4.1. ZMPPT Configuration

If this configuration is selected (see Table 4), the AEM20941 regulates V_{SRC} to be equal to the product of R_{ZMPP} and the available source current. In other terms, the AEM20941 regulates the input impedance of SRC to be equal to R_{ZMPP}.

If unused, leave the resistor footprint R_{ZMPP} empty.

3.4.2. Start-on-Battery Configuration

When the AEM20941 is in DEEP SLEEP MODE (see the "Operating Modes" section from the datasheet), this functionality allows the system to start using the energy from the storage element connected to BATT, instead of cold-starting from the harvester connected to SRC. Therefore, the harvester does not need to match the cold-start constraints to allow for the AEM20941 to start. To do so, a storage element charged to a voltage higher than V_{CHRDY} must be connected to BATT.

To enable this functionality, use a jumper to connect "STONBATT" to "H".

If unused, use a jumper to connect "STONBATT" to "L".

3.4.3. Primary Battery Configuration

If a primary battery is used, it is mandatory to configure $V_{PRIM,MIN}$, the voltage at which the primary battery is considered fully depleted. This configuration is achieved using resistors R7 and R8.

The values of these resistors are determined as follows:

- $R_P = R7 + R8$
- $100k\Omega \leq R_P \leq 500k\Omega$
- $R8 = R_P - R7$
- $R7 = \frac{V_{PRIM\_MIN}}{4} \cdot R_P \cdot \frac{1}{2.2V}$

If unused, use a jumper to short each "NoPRIM" 2-pin headers.

3.4.4. Balancing Circuit Configuration

When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balancing circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two supercapacitor cells to BAL (on BATT connector).
- Use a jumper to connect "BAL" to "ToCN".

See Section 4.5 for an illustration of the AEM20941 balancing circuit behavior.

If storage element balancing is not used, use a jumper to connect "BAL" to "GND".

3.4.5. Ultra-Low Voltage Cold Start Circuit Configuration

The ultra-low voltage cold start (ULVCS) circuit is connected by default on the EVK, and allows for the AEM20941 to coldstart with lower voltage.

The AEM20941 EVK can also be used without the Ultra-Low Voltage Cold Start (ULVCS) circuit, allowing for:

- Lower minimum cold-start conditions, at the expense of a higher minimum cold-start voltage.
- Faster cold-start if conditions without ULVCS are met.
- Lower bill of material (C_{LIN}, C_{OUT}, L_{CS} and D_{CS} are no longer necessary if not using ULVCS).

	Minimum cold-start conditions
With ULVCS	80 mV min. & 650 µA min.
Without ULVCS	380 mV min. & 105 µA min.

Table 5: Cold-start conditions with and without ULVCS

On the AEM20941 EVK, the ULVCS circuit can be disconnected by doing the following:

- Mount a 0 Ω resistor or a solder-bridge on R5 footprint to connect ULVCS_OUT to SRC.
- Remove the 0 Ω resistors R1, R2, R3 and R4.

Copyright © 2025 e-peas SA

4. Functional Tests

Warning regarding measurements

Any item connected to the PCB (load, probe, storage device, etc.) involves a leakage current. This can negatively impact the measurements. Whenever possible, disconnect unused items to limit this effect.

This section presents a few simple tests that allow the user to understand the functional behavior of the AEM20941. To avoid damaging the board, follow the procedure found in Section 3.1 “Safety Information”. If a test has to be restarted make sure to properly reset the AEM20941 to obtain reproducible results (see Section 3.2).

Those functional tests were made using the following setup:

- AEM20941 configuration:
  - SELMPP[1:0] = LL (50%)
  - CFG[2:0] = LHH
    - V_{OVDIS} = 2.80 V
    - V_{CHRDY} = 3.67 V
    - V_{OVCH} = 4.50 V
  - ENHV = H (HVOUT output enabled).
  - ENLV = L (LVOUT output disabled).
- Storage element: see next sections.
- HVOUT: 50 kΩ or floating (see next sections).
- LVOUT left floating.
- SRC: voltage source with series resistor or SMU (see next sections).
- Oscilloscope probes connected to the observed nodes.

NOTE: the setups described in the following sections enable the graphs shown to be reproduced. However, these setups can be adapted to match the user’s application or system, provided that all the constraints from the “Electrical Characteristics at 25 °C” section of the AEM20941 datasheet are met.

Copyright © 2025 e-peas SA

4.1. Start-up

The following test allows users to observe the behavior of the AEM20941 in WAKE-UP MODE.

Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 3.1 “Safety Information”.
- SRC: PSU set as a 2 V voltage source with 2 kΩ series resistor, or SMU set as a 500 µA current source with 2 V voltage compliance. Please note that SRC open-circuit voltage must be higher than 80 mV to allow for the AEM20941 to coldstart.
- BATT: 330 µF electrolytic capacitor in parallel with the on-board C_{BATT}. BAL is connected to GND.

Observations and Measurements

Referring to Figure 3:

- Switch on SRC PSU and let the AEM20941 coldstart.
- SRC is then regulated at V_{MPP} as shown on Figure 4, which is a voltage equal to the open-circuit voltage (V_{OC}) multiplied by the MPPT ratio (here 50%). During the MPPT evaluation, the AEM20941 stops pulling current from SRC, letting V_{SRC} rise to V_{OC}.
- BATT voltage rises as the power provided by the source is transferred to the storage element.
- When BATT voltage first reaches V_{CHRDY}, HVOUT starts being supplied and is regulated according to the configuration of CFG[2:0]. STATUS[0] is also asserted at that moment. The behavior of LVOUT would be the same as that of HVOUT if the ENLV pin is set to “H”.

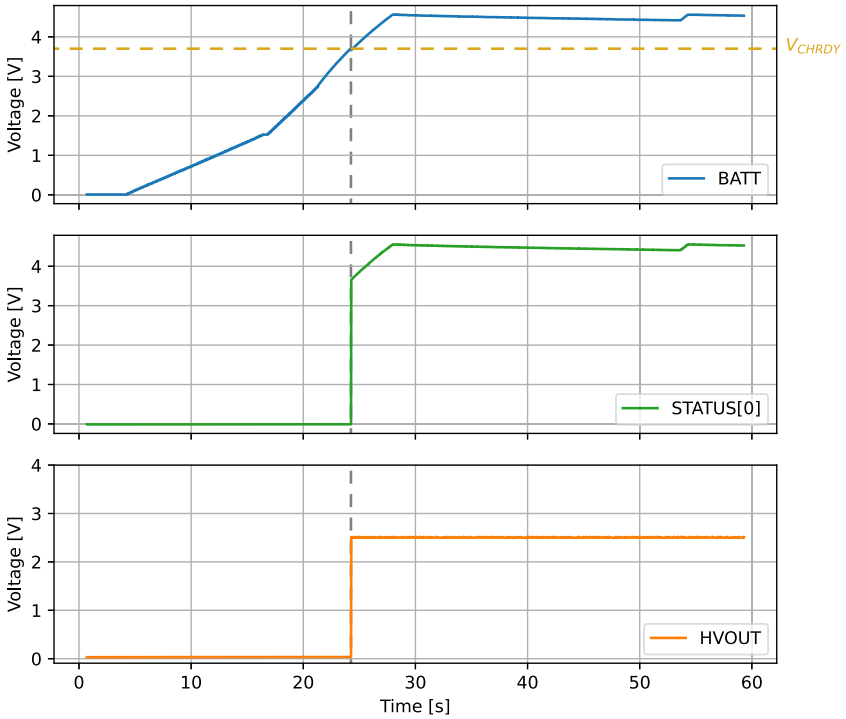


Figure 3: STATUS[0] and HVOUT evolution with BATT

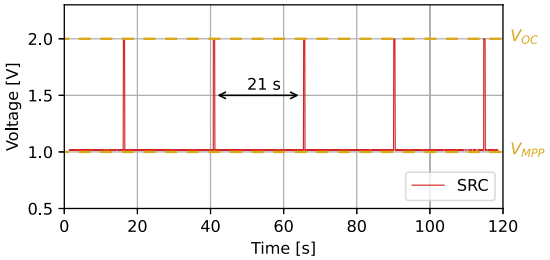


Figure 4: SRC voltage behavior while harvesting (BATT voltage under V_{OVCH})

Copyright © 2025 e-peas SA

4.2. Shutdown

This test allows users to observe the behavior of the AEM20941 when the system is running out of energy.

Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 3.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 4.1). Do not connect a primary battery.
- SRC: any suitable power source to make the AEM20941 coldstart and reach a steady state (for example a PSU set as a 1.0 V voltage source with a 100 Ω series resistor).
- Let the system reach a steady state (i.e. voltage on BATT between V_{CHRDY} and V_{OVCH}, and STATUS[0] asserted). A 330 µF capacitor is connected between BATT and GND, in parallel with the on-board C_{BATT} capacitor.
- Switch off the source and allow the system to discharge through quiescent current and any load(s) connected to HVOUT/LVOUT. A 50 kΩ load was connected to HVOUT to create the graphs shown on Figure 5.

Observations and Measurements

Referring to Figure 5:

- BATT voltage decreases as the system consumes the energy from the storage element.
- When BATT voltage drops below V_{OVDIS}, STATUS[1] is asserted during 600 ms.
- 600 ms after crossing V_{OVDIS}, the storage element is no longer discharged as HVOUT, with its 50 kΩ load, is no longer supplied, so BATT voltage then remains stable. At that moment, STATUS[0] and STATUS[1] are both de-asserted. Figure 5 shows only the behavior of HVOUT, but LVOUT behaves the same in those conditions.

NOTE: STATUS[1] might be used to notify the application circuit that the storage element is over-discharged and that HVOUT and LVOUT will no longer be supplied within 600 ms.

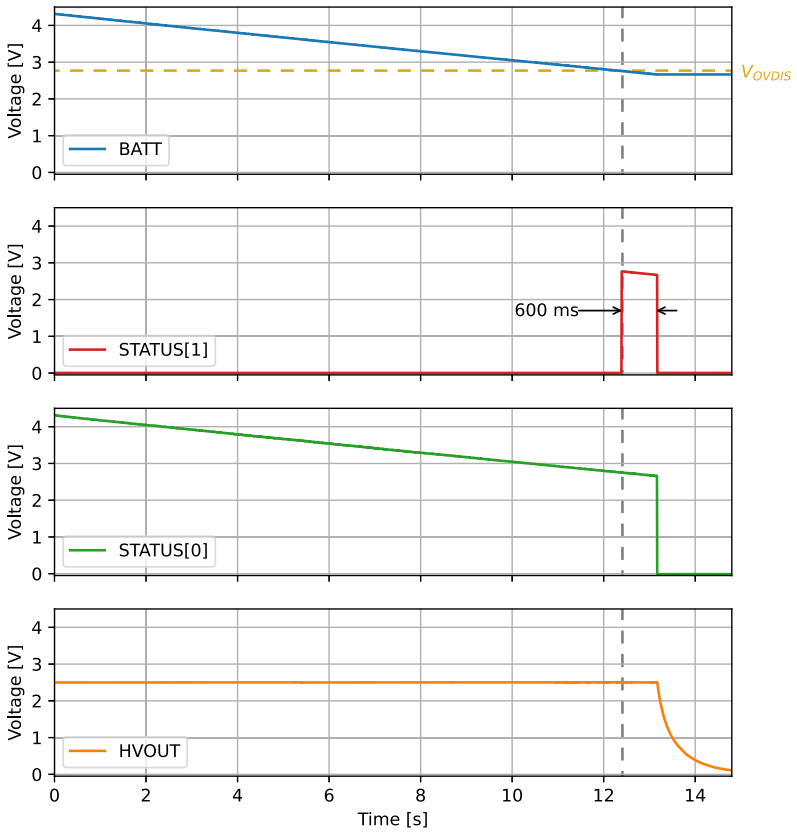


Figure 5: AEM20941 shutdown behavior

Copyright © 2025 e-peas SA

4.3. Primary Battery

This test allows users to observe the AEM20941 recharging the storage element (BATT) from the primary battery when the system is running out of energy.

Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 3.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 4.1).
- PRIM: simulated by a 3 V voltage source (PSU) with 200 Ω series resistor. The primary battery discharge protection level $V_{PRIM,MIN}$ set to 2.4 V, with R7 = 68 kΩ and R8 = 180 kΩ. Please note that the user must remove jumpers from both “NoPRIM” headers before connecting the primary battery.
- SRC: any suitable power source to make the AEM20941 coldstart and reach a steady state (for example a PSU set as a 1.0 V voltage source with a 100 Ω series resistor).
- HVOUT: 50 kΩ resistor connected between HVOUT and GND.
- Let the system reach a steady state (i.e. voltage on BATT between V_{CHRDY} and V_{OVCH}, and STATUS[0] asserted).
- Remove the source and let the system discharge through the 50 kΩ load connected to HVOUT and through the AEM20941 quiescent current.

Observations and Measurements

Referring to Figure 6:

- BATT voltage decreases as the system consumes energy from the storage element, mainly due to the 50 kΩ load connected to HVOUT.
- When BATT voltage drops below V_{OVDIS}, the AEM20941 extracts energy from the primary battery, recharging BATT until its voltage rises above V_{CHRDY}. STATUS[1] is asserted while the AEM20941 pulls current from the primary battery.
- HVOUT remains stable and unaffected by the storage element reaching V_{OVDIS}, as it is automatically recharged from the primary battery. STATUS[0] stays asserted.

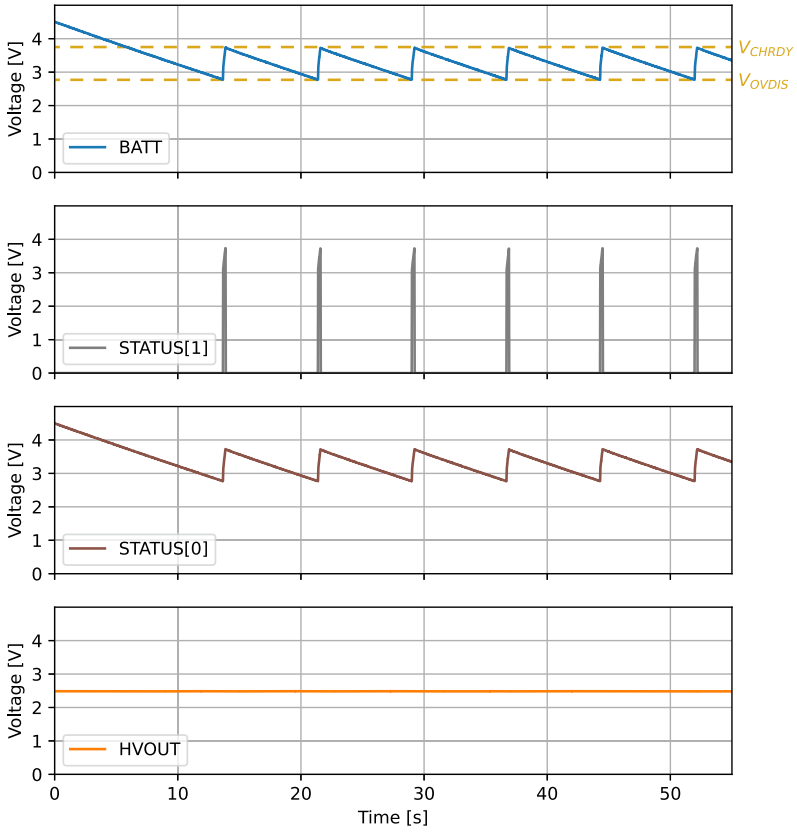


Figure 6: Recharging BATT from the primary battery

Copyright © 2025 e-peas SA

4.4. Cold Start

The following test allows the user to observe that the AEM20941 is able to coldstart even from a very low voltage. The user should avoid probing any unnecessary node to prevent excessive leakage caused by the probes. It is essential to properly reset the board before the test in order to observe the cold-start behavior.

Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 3.1 “Safety Information”. Configure the board in the desired state (see Section 4.1).
- SRC: 0.5 V voltage source (PSU) with a 100 Ω series resistor. This setting makes it easy to differentiate the cold-start voltage (here about 60 mV) from the MPP voltage (V_{MPP}), which is 50 % of 500 mV (250 mV).
- BATT: 330 µF capacitor in parallel with the on-board C_{BATT} capacitor.

Observations and Measurements

Referring to Figure 7:

- The SRC voltage V_{SRC} is clamped to the cold-start voltage during the cold-start phase, which ends when BUCK voltage reaches about 1.8 V.
- A first open-circuit voltage evaluation is performed.
- V_{SRC} is then regulated at the ratio of V_{OC}, as selected by the user with the SELMPP[1:0] pins. Please note that, during the initial open-circuit voltage evaluation, the time allowed by the AEM20941 for the harvester to reach its open-circuit voltage is very short, resulting in an approximate MPP voltage. The next open-circuit voltage evaluation occurs after $T_{MPPT,PERIOD}$ / 2. All subsequent MPP evaluations comply with the $T_{MPPT,PERIOD}$, $T_{MPPT,WAIT}$ and $T_{MPPT,MEASURE}$ values specified in the datasheet.
- The storage element connected to BATT starts to charge as soon as the cold-start phase is over.
- The voltage peaks observed on the SRC pin during the first part of WAKE-UP MODE are due to C_{BOOST} being discharged several times in the storage element, as described in the datasheet “Deep Sleep & Wake Up Modes” section.
- Please note that the cold-start duration decreases as the input power increases, so its observation is easier with low source power.

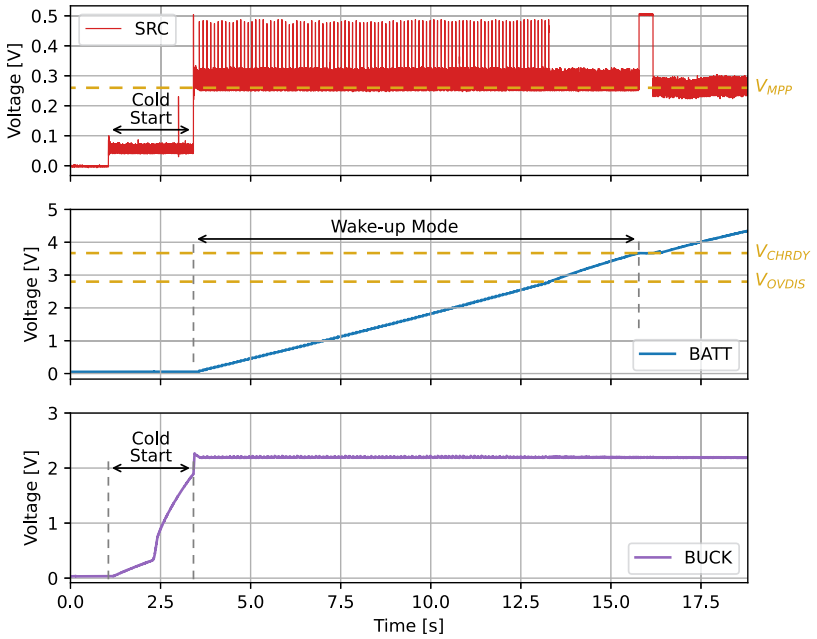


Figure 7: AEM20941 behavior during cold start

Copyright © 2025 e-peas SA

4.5. Dual-cell Supercapacitor Balancing Circuit

When using a dual-cell supercapacitor as storage element, it is necessary to keep both cells at similar voltages to avoid damage due to a potential over-voltage on one cell, which could happen if both cells do not have the exact same capacitance. This is ensured by the AEM20941 storage element balancing circuit (BAL pin).

The following test allows the user to observe the balancing circuit behavior. In this example, a mismatched dual-cell supercapacitor is simulated by using a 470 µF capacitor in series with a 330 µF capacitor, but any couple of capacitors could be used as long as the resulting capacitance seen by BATT matches the values specified in the "Recommended Operating Conditions" section from the AEM20941 datasheet. The capacitance mismatch must also be realistic, with a maximum factor of 2 between the top and the bottom capacitor (see Figure 8). Please note that the balancing circuit in enabled only if the voltage on the BAL pin is above $V_{BAL,MIN}$ (0.9 V). Please note that those capacitors are also in parallel with the on-board C_{BATT} capacitor, which can be seen on the EVK schematic (Figure 15).

Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 3.1 "Safety Information". Configure the board in the desired state (see Section 4.1). Install a jumper linking BAL to "ToCN".
- BATT: as shown on Figure 8, connect C_{TOP} between BATT and BAL, and C_{BOT} between BAL and GND.

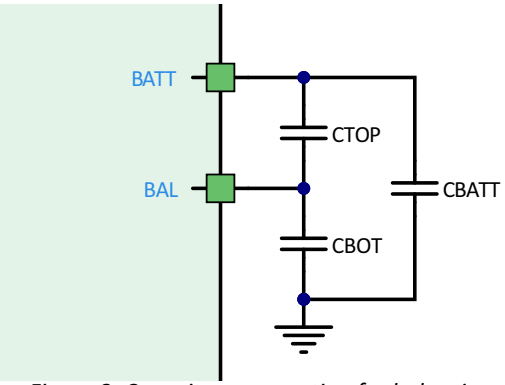


Figure 8: Capacitors connection for balancing

- SRC: connect the source element to power up the system. On Figure 9, Figure 10 and Figure 11, a PSU was used, set as a 1 V voltage source with a 100 Ω series resistor between the PSU positive terminal and the AEM20941 SRC pin.
- No load on HVOUT.

Observations and Measurements

- As a reference, Figure 9 shows the behavior of charging a mismatched dual-cell (super)capacitor without the balancing circuit. C_{TOP} (330 µF) and C_{BOT} (470 µF) are in series and connected between BATT and GND. The balancing functionality is disabled by connecting BAL to GND, ensuring that BAL voltage is below $V_{BAL,MIN}$ (0.9 V). The graph shows that balancing between C_{TOP} and C_{BOT} is not maintained: the voltage at C_{TOP}-C_{BOT} midpoint is significantly lower than half BATT voltage, meaning that the voltage across C_{TOP} is higher than the one across C_{BOT}.

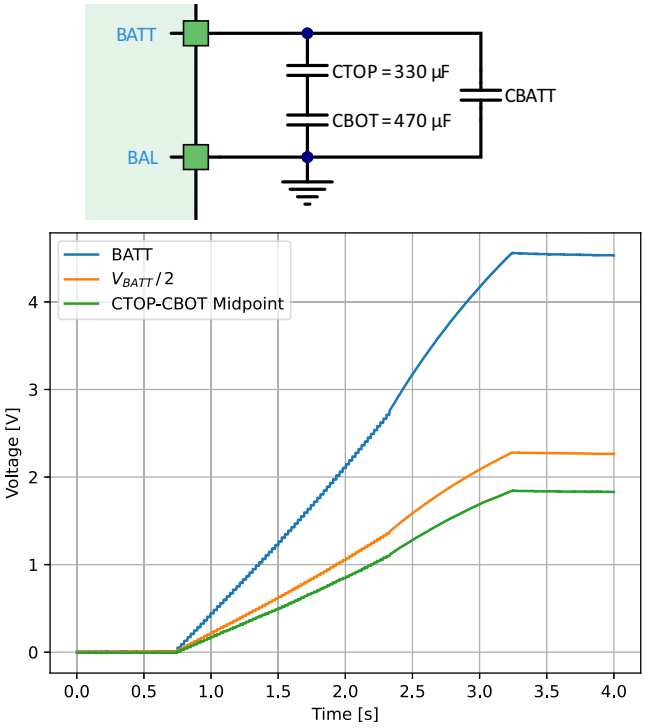


Figure 9: Dual-cell (super)capacitor schematic and charging behavior without the balancing circuit

Copyright © 2025 e-peas SA

- Figure 10: the capacitance of C_{BOT} is smaller than the one of C_{TOP}, so C_{BOT} charges faster than C_{TOP}. The balancing circuit starts to work when the voltage on BAL reaches $V_{BAL,MIN}$ (0.9 V). At 1.5 s, the balancing circuit starts and C_{BOT} is kept at $V_{BAL,MIN}$ until C_{TOP} is sufficiently charged for the BAL voltage to sit at half the BATT voltage. The balancing circuit then regularly discharges C_{BOT} to maintain the balancing of C_{BOT} and C_{TOP}. This creates small voltage drops on both BATT and BAL. BAL voltage is always kept close to half of BATT voltage.

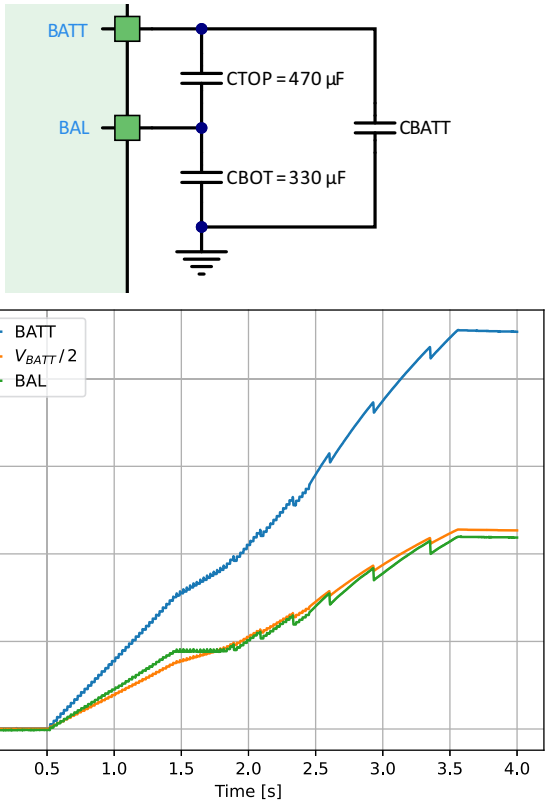


Figure 10: Balancing circuit schematic and behavior (C_{TOP} > C_{BOT})

- Figure 11: the capacitance of C_{TOP} is now smaller than the one of C_{BOT}, so that C_{TOP} charges faster than C_{BOT}. When the BAL pin reaches $V_{BAL,MIN}$ (0.9 V), C_{TOP} is discharged into C_{BOT}, reducing C_{TOP} voltage and thus maintaining the balance between C_{TOP} and C_{BOT} voltages. This happens then regularly, so that BAL voltage is always kept close to half of BATT voltage, keeping the voltage on both capacitors close as well.

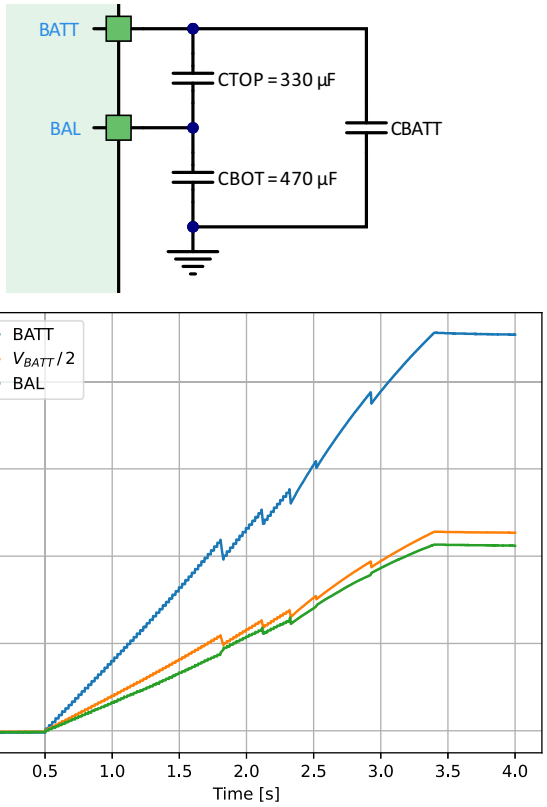


Figure 11: Balancing circuit schematic and behavior (C_{BOT} > C_{TOP})

Copyright © 2025 e-peas SA

5. Performance Tests

This section presents the tests to reproduce the performance graphs found in the AEM20941 datasheet and to understand the functionalities of the AEM20941. To be able to reproduce those tests, the following equipment is required:

- 1 voltage source.
- 2 source measure units (SMUs).
- 1 oscilloscope.

An SMU is a costly equipment, so alternatives are suggested when possible.

To avoid damaging the board, follow the procedure in Section 3.1 “Safety Information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results (see “How to reset the AEM20941 evaluation board” in Section 3.2).

5.1. LDOs Load and Line Regulation

The following test allows for evaluating the output voltage stability of the LDOs (HVOUT / LVOUT pins) with various storage element voltages (BATT pin). See the “Typical Characteristics” section of the AEM20941 datasheet.

Setup

- Reset the EVK following the protocol described in Section 3.2. Referring to Figure 1, configure the board to the desired state.
- BATT: connect either a power supply (PSU) or an SMU on the BATT pin:
  - SMU: configured as a voltage source with a 100 mA current compliance.
  - PSU: configured as a voltage source with 100 mA current compliance. Connect a parallel 100 Ω resistor between the positive and the negative terminal to allow for sinking the current provided by the SRC pin through the boost converter. Ensure the resistor’s power rating is sufficient to dissipate the power provided by the PSU.
- SRC: connect either a PSU or an SMU on the SRC pin. The SRC connection is only necessary for the AEM20941 to coldstart, so its regulation voltage setting does not matter as long as the voltage/ current are both above the cold-start conditions.
  - PSU: configured as a 1 V voltage source with a 10 mA current compliance, with a 100 Ω resistor in series.
  - SMU: configured as 2.5 mA current source with 1.0 V voltage compliance.
- HVOUT / LVOUT: connect either an SMU or a resistor to HVOUT / LVOUT:
  - SMU: configured as a 0 V voltage source with current compliance set to the desired load current. The SMU absorbs the current provided by the LDO, while the voltage is imposed by the LDO regulation target voltage. The maximum current that can be sourced by each LDO is defined in “Electrical Specifications at 25°C” section of the AEM20941 datasheet.
  - Resistor: set the value to achieve the desired load current (I = U / R). Ensure the resistor’s power rating is sufficient to dissipate the power provided by HVOUT / LVOUT.

Manipulations

- Apply a voltage above V_{OVCH} on the BATT pin (make sure to comply to the values defined in the “Absolute Maximum Ratings” from the AEM20941 datasheet).
- While keeping the voltage above V_{OVCH} on BATT, switch on the PSU/SMU on SRC to coldstart the AEM20941.
- Sweep voltage on BATT from V_{OVDIS} + 50 mV to 4.5 V.
- Repeat with different load currents:
  - HVOUT: from 10 µA to 80 mA.
  - LVOUT: from 10 µA to 20 mA.

Measurements

- Measure the voltage on HVOUT / LVOUT to observe the LDOs voltage regulation. Typical results are shown on Figure 12 and Figure 13.

Copyright © 2025 e-peas SA

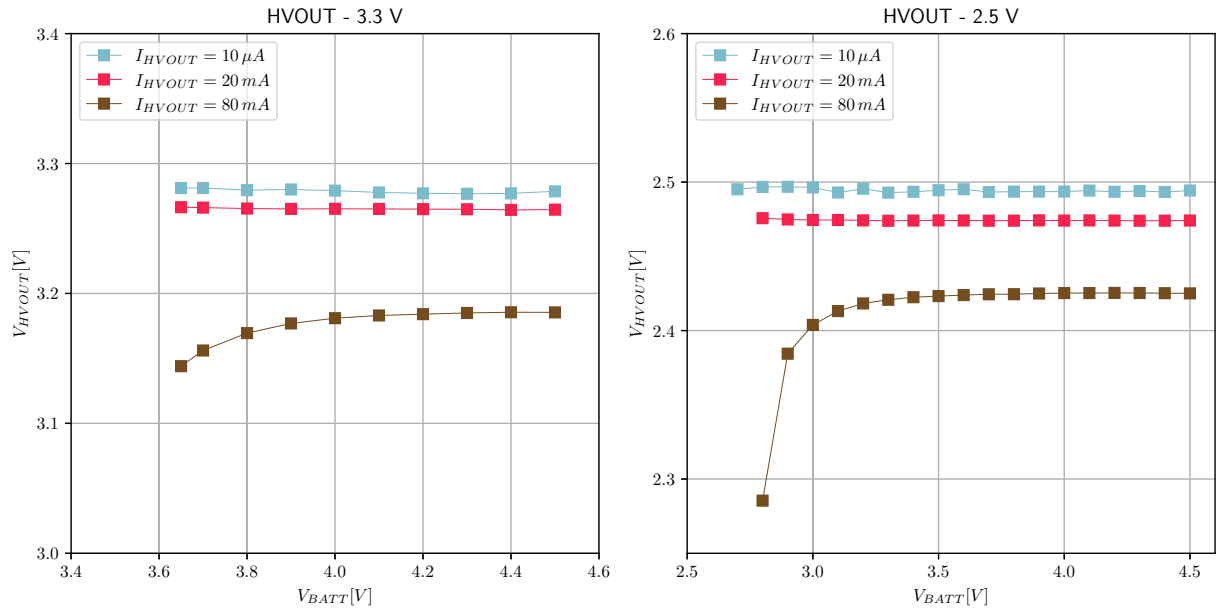


Figure 12: HVOUT at 3.3 V and 2.5 V

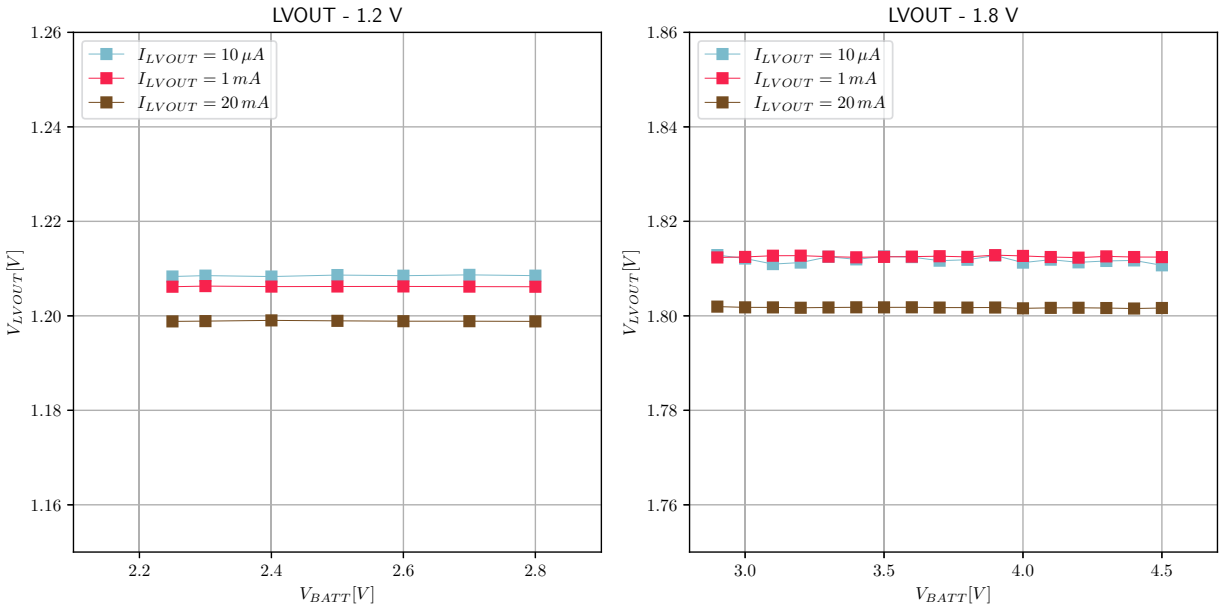


Figure 13: LVOUT at 1.2 V and 1.8 V

Copyright © 2025 e-peas SA

5.2. Boost Converter Efficiency

This test enables users to recreate the efficiency graphs of the AEM20941 boost converter ("Boost Conversion Efficiency for LBOOST = 10 µH" section of the AEM20941 datasheet). Please note that in NORMAL MODE, pins BATT and BOOST are connected, so monitoring either one is fine for that test.

Setup

- Following steps 1 and 2 explained in the Section 3.1 and referring to Figure 1, configure the board in the desired state.
- BATT: connect an SMU configured as a voltage source. Set the current compliance and range high enough to prevent the SMU from hitting the current compliance and ensure valid measurement, but not too high to preserve accuracy.
- SRC: connect an SMU configured as a 1 mA current source. Start with a voltage compliance of 1 V for the AEM20941's cold start.

Manipulations

- Set a voltage between V_{OVCH} and 5 V on the BATT SMU and switch on the SRC SMU to coldstart the AEM20941. When done, impose a voltage between V_{OVDIS} + 50 mV and V_{OVCH} on the BATT SMU.
- Sweep voltage compliance on the SRC SMU from $V_{SRC,MIN}$ to 4.5 V.
- Repeat with different current levels on the SRC SMU (from 100 µA to 100 mA) and with different voltage levels on the BATT SMU (from V_{OVDIS} + 50 mV to V_{OVCH}). Make sure that the measurement takes place to capture at least 20 MPPT cycles (420 s for the AEM20941).
- Read the average voltage and current values on both SMUs to determine the efficiency.

Measurements

- Clear both SMU buffer before starting each measurement point.
- SRC: measure the average current and voltage.
- BATT: measure the average current and voltage.
- The measurement must last long enough for the average values read on both SMUs to be stable. Figure 14 has been obtained by averaging over 100 measurements configured with a 200 ms integration time.
- Determine the efficiency η as follows:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}}$$

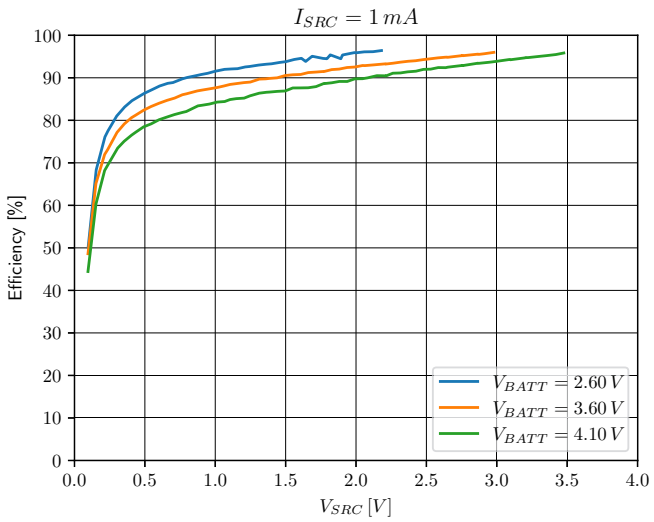


Figure 14: Boost efficiency for I_{SRC} = 1mA, L_{BOOST} = 10 µH (Coilcraft LPS4018-103)

Copyright © 2025 e-peas SA

6. Schematic

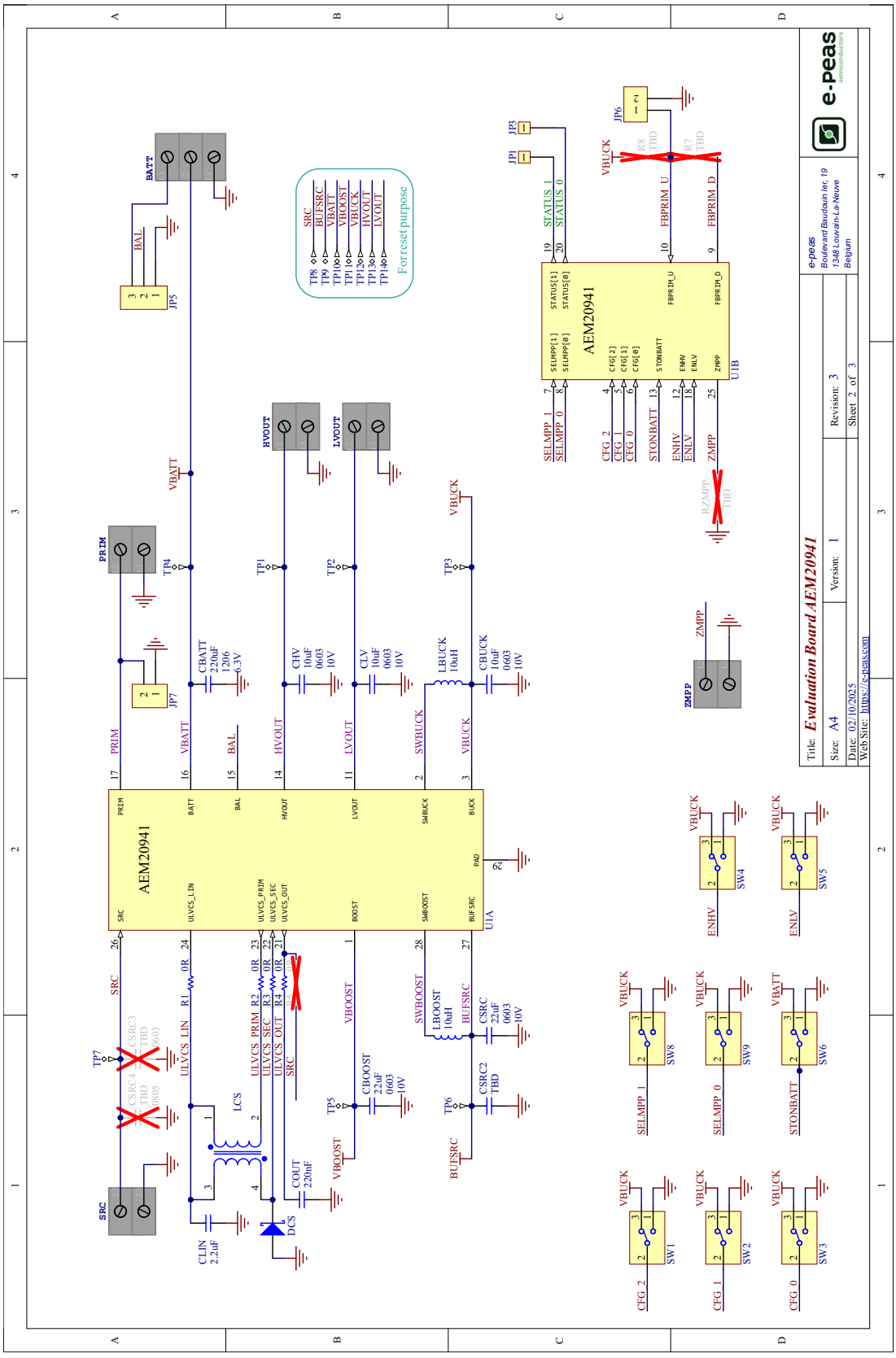


Figure 15: AEM20941 evaluation board schematic

Copyright © 2025 e-peas SA

7. Revision History

EVK Version	User Guide Revision	Date	Description
1.2	1.0	October, 2025	Creation of the document.
1.3	1.0	December, 2025	- Updated document for EVK v1.3. - Added “Ultra-Low Voltage Cold Start Circuit Configuration” section.

Table 6: Revision history

Copyright © 2025 e-peas SA