AEM00330 Evaluation Board User Guide

Description

The AEM00330 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM00330 integrated circuit (IC).

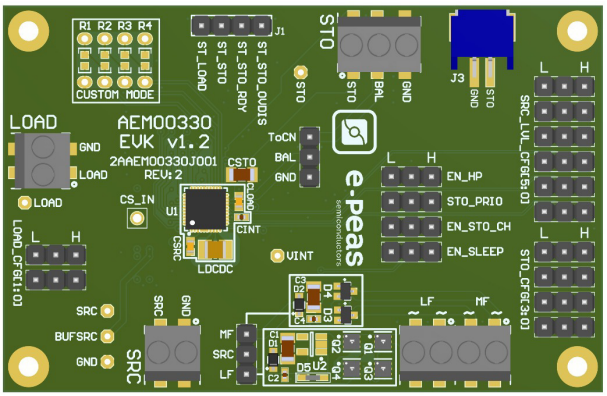
The AEM00330 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting.

It allows easy connections to the energy harvester, the storage element and the load. It also provides all the configuration access to set the device in any one of the modes described in the datasheet. The control and status signals are available on standard pin headers, allowing users to wire for any usage scenario and evaluate the relevant performances.

The AEM00330 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes, etc.) for the design of a highly efficient subsystem in your target application.

More detailed information about AEM00330 features can be found in the datasheet.

Appearance



Features

Four two-way screw terminals

- Source of energy (DC).
- Source of energy (AC low frequency).
- Source of energy (AC medium frequency).
- Load.

One three-way screw terminal

- Energy storage element (battery or (super)capacitor).

One 2-pin “Shrouded Header”

- Alternative connector for the storage element.

3-pin headers

- Source voltage regulation configuration (SRC_LVL_CFG).
- Storage element voltage configuration.
- Load voltage configuration.
- Dual-cell supercapacitor configuration.
- Modes configuration.

Provision for resistors

- Custom mode configuration.

Configuration by 0 Ω resistors

- Cold start input configuration.

Four 1-pin headers

- Access to status pins.

Device Information

Part Number	Dimensions
2AAEM00330J001	76 mm x 50 mm

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1. Connections Diagram

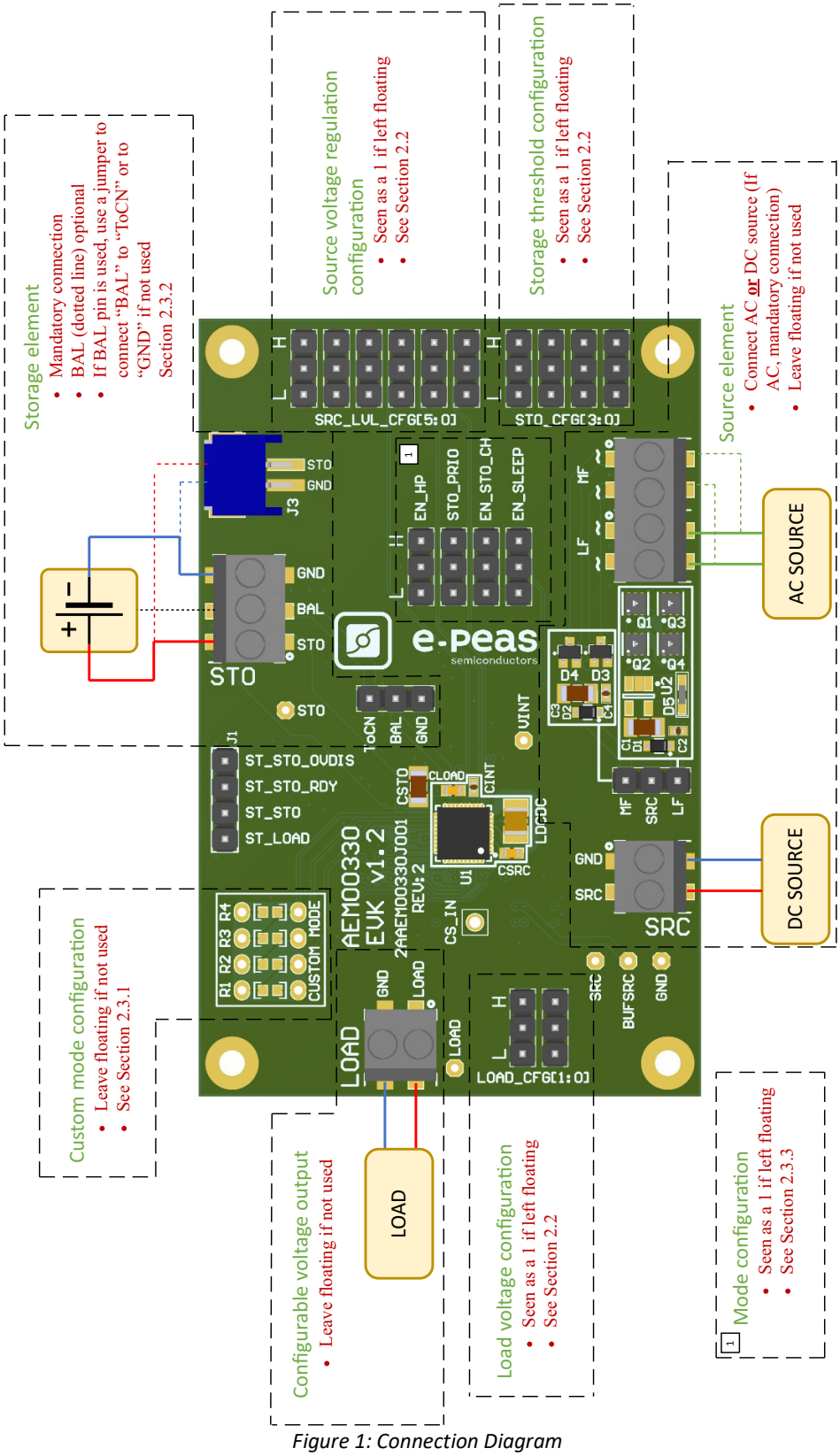

Figure 1: Connection Diagram

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1.1. Signals Description

NAME	FUNCTION	CONNECTION	
		If used	If not used
Power signals			
SRC	Connection to the harvested energy source.	Connect the source element.	
STO	Connection to the energy storage element.	Connect the storage element in addition to CSTO (150 µF).	Do not remove CSTO.
BAL	Connection to mid-point of the dual-cell supercapacitor.	Connect balancing and place a jumper shorting "BAL" and "ToCN".	Use a jumper to connect "BAL" to "GND".
LOAD	Connection to the load (Application).	Connect a load.	Leave floating.
LF	Connection to the AC harvested energy source. (Low frequency).	Connect the source element.	Leave floating.
MF	Connection to the AC harvested energy source. (Medium frequency).	Connect the source element.	Leave floating.
Debug signals			
VINT	Internal voltage supply.		
BUFSRC	Connection to an external capacitor buffering the buck-boost converter input.		
Configuration signals			
SRC_LVL_CFG[5:0]	Configuration of the source voltage regulation.	Connect jumpers.	
STO_CFG[3:0]	Configuration of the threshold voltages for the energy storage element.	Connect jumpers.	Leave floating.
LOAD_CFG[1:0]	Configuration of the load voltage.	Connect jumpers.	
Control signals			
EN_HP	Enabling pin for the high-power mode.	Connect jumper.	
STO_PRIO	Pin for the storage/load priority.	Connect jumper.	
EN_STO_CH	Enabling pin for the storage charging.	Connect jumper.	
EN_SLEEP	Enabling pin for the sleep mode.	Connect jumper.	Can't be left floating.
Status Signals			
ST_LOAD	Logic output. Asserted when the LOAD voltage rises above the $V_{LOAD,TYP}$ threshold. Reset when the LOAD voltage drops below $V_{LOAD,MIN}$ threshold. High level is V_{LOAD}.		
ST_STO	Logic output. Asserted when the storage device voltage rises above the V_{CHRDY} threshold. Reset when the storage device voltage drops below V_{OVDIS} threshold. High level is V_{STO}.		
ST_STO_RDY	Logic output. Asserted when the storage element is above V_{CHRDY}. High level is V_{LOAD}.		
ST_STO_OVDIS	Logic output. Asserted when the storage element voltage V_{STO} drops below V_{OVDIS}. High level is V_{LOAD}.		

Table 1: Signals Description

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2. General Considerations

2.1. Safety Information

Always connect the elements in the following order:

1. Reset the board: Short VINT, LOAD, STO and SRC test points to GND.
2. Completely configure the PCB (jumpers/resistors):
   - Source voltage regulation configuration.
   - Battery configuration.
   - Load voltage configuration.
   - Balancing circuit configuration.
   - Mode configuration.
3. Connect the storage elements on STO.
4. Connect the Load on LOAD.
5. Connect the source (DC or AC) to the SRC connector.

To avoid damaging the board, users are required to follow this procedure.

The pins “BAL” and EN_SLEEP cannot remain floating.

2.2. Basic Configurations

Configuration pins				Storage element threshold voltages			Typical use
STO_CFG[3:0]				V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
L	L	L	L	3.00 V	3.50 V	4.05 V	Li-ion battery
L	L	L	H	2.80 V	3.10 V	3.60 V	LiFePO4 battery
L	L	H	L	1.85 V	2.40 V	2.70 V	Dual-cell NiMH battery
L	L	H	H	0.20 V	1.00 V	4.65 V	Dual-cell supercapacitor
L	H	L	L	0.20 V	1.00 V	2.60 V	Single-cell supercapacitor
L	H	L	H	1.00 V	1.20 V	2.95 V	Single-cell supercapacitor
L	H	H	L	1.85 V	2.30 V	2.60 V	NGK
L	H	H	H	Custom Mode (single-cell NiMH, LiC, etc.)			
H	L	L	L	1.10 V	1.25 V	1.50 V	Ni-Cd 1 cells
H	L	L	H	2.20 V	2.50 V	3.00 V	Ni-Cd 2 cells
H	L	H	L	1.45 V	2.00 V	4.65 V	Dual-cell supercapacitor
H	L	H	H	1.00 V	1.20 V	2.60 V	Single-cell supercapacitor
H	H	L	L	2.00 V	2.30 V	2.60 V	Micro batteries
H	H	L	H	3.00 V	3.50 V	4.35 V	Li-Po battery
H	H	H	L	2.60 V	2.70 V	4.00 V	Tadiran TLI1020A
H	H	H	H	2.60 V	3.50 V	3.90 V	Tadiran HLC1020

Table 2: Storage Element Configuration Pins

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Configuration pins		LOAD output voltage			
LOAD_CFG[1:0]		$V_{LOAD,MIN}$	$V_{LOAD,MID}$	$V_{LOAD,TYP}$	$V_{LOAD,MAX}$
L	L	3.15 V	3.23 V	3.28 V	3.34 V
L	H	2.35 V	2.47 V	2.50 V	2.53 V
H	L	1.64 V	1.75 V	1.79 V	1.82 V
H	H	1.14 V	1.16 V	1.20 V	1.23 V

Table 3: Load Configuration Pins

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
L	L	L	L	L	L	0.14 V
L	L	L	L	L	H	0.17 V
L	L	L	L	H	L	0.20 V
L	L	L	L	H	H	0.23 V
L	L	L	H	L	L	0.26 V
L	L	L	H	L	H	0.30 V
L	L	L	H	H	L	0.34 V
L	L	L	H	H	H	0.39 V
L	L	H	L	L	L	0.43 V
L	L	H	L	L	H	0.48 V
L	L	H	L	H	L	0.52 V
L	L	H	L	H	H	0.57 V
L	L	H	H	L	L	0.61 V
L	L	H	H	L	H	0.66 V
L	L	H	H	H	L	0.70 V
L	L	H	H	H	H	0.75 V
L	H	L	L	L	L	0.80 V
L	H	L	L	L	H	0.84 V
L	H	L	L	H	L	0.89 V
L	H	L	L	H	H	0.95 V
L	H	L	H	L	L	1.05 V
L	H	L	H	L	H	1.14 V
L	H	L	H	H	L	1.23 V
L	H	L	H	H	H	1.32 V
L	H	H	L	L	L	1.41 V
L	H	H	L	L	H	1.50 V
L	H	H	L	H	L	1.59 V
L	H	H	L	H	H	1.68 V
L	H	H	H	L	L	1.77 V
L	H	H	H	L	H	1.86 V

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
L	H	H	H	H	L	1.95 V
L	H	H	H	H	H	2.05 V
H	L	L	L	L	L	2.14 V
H	L	L	L	L	H	2.23 V
H	L	L	L	H	L	2.32 V
H	L	L	L	H	H	2.41 V
H	L	L	H	L	L	2.50 V
H	L	L	H	L	H	2.59 V
H	L	L	H	H	L	2.68 V
H	L	L	H	H	H	2.77 V
H	L	H	L	L	L	2.86 V
H	L	H	L	L	H	2.95 V
H	L	H	L	H	L	3.05 V
H	L	H	L	H	H	3.14 V
H	L	H	H	L	L	3.23 V
H	L	H	H	L	H	3.32 V
H	L	H	H	H	L	3.41 V
H	L	H	H	H	H	3.50 V
H	H	L	L	L	L	3.59 V
H	H	L	L	L	H	3.68 V
H	H	L	L	H	L	3.77 V
H	H	L	L	H	H	3.86 V
H	H	L	H	L	L	3.95 V
H	H	L	H	L	H	4.05 V
H	H	L	H	H	L	4.14 V
H	H	L	H	H	H	4.23 V
H	H	H	L	L	L	4.32 V
H	H	H	L	L	H	4.41 V
H	H	H	L	H	L	4.50 V

Table 4: Source Regulation Configuration Pins

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2.3. Advanced Configurations

A complete description of the system constraints and configurations is available in the AEM00330 datasheet "System Configuration" Section.

A reminder on how to calculate the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found on the e-peas website.

2.3.1. Custom Mode

In addition to the pre-defined protection levels, the custom mode allows users to define their own levels via resistors R1 to R4, according to the following equations:

- $R_T = R_1 + R_2 + R_3 + R_4$
- $1M\Omega \leq R_T \leq 100M\Omega$
- $R_1 = R_T \cdot \frac{1V}{V_{OVCH}}$
- $R_2 = R_T \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}}\right)$
- $R_3 = R_T \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}}\right)$
- $R_4 = R_T \cdot \left(1 - \frac{1V}{V_{OVDIS}}\right)$

User must ensure that the protection levels satisfy the following conditions:

- $V_{CHRDY} + 0.05V \leq V_{OVCH} \leq 4.5V$
- $V_{OVDIS} + 0.05V \leq V_{CHRDY} \leq V_{OVCH} - 0.05V$
- $1V \leq V_{OVDIS}$

If unused, leave the resistor footprints (R1 to R4) empty.

2.3.2. Balancing Circuit Configuration

When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balancing circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two supercapacitor cells to BAL (on STO connector).
- Use a jumper to connect "BAL" to "ToCN".

If unused, use a jumper to connect "BAL" to "GND".

2.3.3. Mode Configuration

EN_HP

When EN_HP is pulled up to VINT, the DCDC converter is set to HIGH POWER MODE. This allows higher currents to be extracted from the buck-boost input (SRC or STO) to the buck-boost output (LOAD, STO or VINT).

- Use a jumper to connect EN_HP to H to enable the high-power mode.
- Use a jumper to connect EN_HP to L to disable the high-power mode.

STO_PRIO

It is possible to define a priority between STO and LOAD.

- Use a jumper to connect the STO_PRIO to H to supply the storage element to V_{CHRDY} before start supplying the LOAD.
- Use a jumper to connect the STO_PRIO to L to supply in the first place the LOAD, charging the storage element with the remaining energy.

EN_STO_CH

To disable battery charging, the 3-pin header is available.

- Use a jumper to connect the EN_STO_CH to H to enable the charge of the storage element.
- Use a jumper to connect the EN_STO_CH to L to disable the charge of the storage element.

An internal pull-up resistor is setting the EN_STO_CH at H by default.

EN_SLEEP

The SLEEP STATE reduces the AEM00330 quiescent current by ceasing the energy extraction from the SRC and reducing V_{LOAD} and V_{VINT} monitoring period.

- Use a jumper to connect the EN_SLEEP to H to activate the feature.
- Use a jumper to connect the EN_SLEEP to L to disable the feature.

Do not leave EN_SLEEP floating, doing so could damage the AEM.

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3. Functional Tests

This section presents a few simple tests that allow the user to understand the functional behavior of the AEM00330. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted make sure to properly reset the system to obtain reproducible results.

The following functional tests were made using the following setup:

- SRC_LVL_CFG[5:0] = LHHLLH.
- STO_CFG[3:0] = LLLL.
- EN_HP = H.
- STO_PRIO = H.
- EN_STO_CH = H.
- EN_SLEEP = L.
- Storage element: Capacitor (4.7 mF + CSTO).
- Load: 10kOhm on LOAD.
- SRC: current source (1mA or 100uA) with voltage compliance (4V).

Setup can be adapted to match user’s system as long as the input and cold-start constraints are met (see the AEM00330 datasheet “Introduction” Section).

3.1. Start-up

The following example allows the user to observe the behavior of the AEM00330 in Wake-up state.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.

Observations and Measurements

- STO: Voltage rises as the power provided by the source is transferred to the storage element.
- LOAD: Regulated when voltage on STO first rises above V_{CHRDY}.
- ST_LOAD: Asserted when LOAD is supplied.
- ST_STO and ST_STO_RDY: Asserted when the voltage on STO rises above V_{CHRDY}.

3.2. Shutdown

This test allows users to observe the behavior of the AEM00330 when the system is running out of energy.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- Let the system reach a steady state (i.e. voltage on STO between V_{CHRDY} and V_{OVCH} and ST_STO asserted.
- Remove your source element and let the system discharge through quiescent current and load.

Observations and Measurements

- STO: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches V_{OVDIS}.
- ST_STO_RDY: De-asserted when the voltage on STO goes below V_{CHRDY}.
- ST_LOAD: De-asserted when the load is no longer available.
- ST_STO_OVDIS: Asserted for 680 ms when the storage element voltage (STO) falls below V_{OVDIS}.
- ST_STO: De-asserted when the storage element is running out of energy (V_{OVDIS}).

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3.3. Cold Start

The following test allows the user to observe the minimum voltage required to coldstart the AEM00330. To prevent leakage current induced by the probe the user should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behavior.

Setup

- Place the probes on the nodes to be observed.
- Referring Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Do not plug any storage element in addition to CSTO.
- SRC: Connect your source element.

Observations and Measurements

- SRC: Equal to the cold-start voltage during the cold-start phase. Regulated at the source voltage configured thanks to SRC_LVL_CFG[5:0] when cold start is over. Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.
- STO: Starts to charge the storage element when the cold-start phase is over.

3.4. Dual-cell Supercapacitor Balancing Circuit

This test allows users to observe the balancing circuit behavior that maintains the voltage on BAL at half the voltage on STO.

Setup

- Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state. Plug the jumper linking “BAL” to “ToCN”.
- STO: Connect capacitor C1 between the positive (+) and the BAL pins and a capacitor C2 between BAL and the negative (-) pins. Select C1 and C2 so that:
  - $C1 \neq C2$
  - $C1 > 1mF$
  - $C2 > 1mF$
  - $\frac{C2 \cdot V_{CHRDY}}{C1} \geq 0.9V$
- SRC: Plug your source element to start the power flow to the system.

Observations and Measurements

- BAL: Equals to half the voltage on STO.

Do not leave BAL floating, doing so could damage the AEM.

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4. Schematics

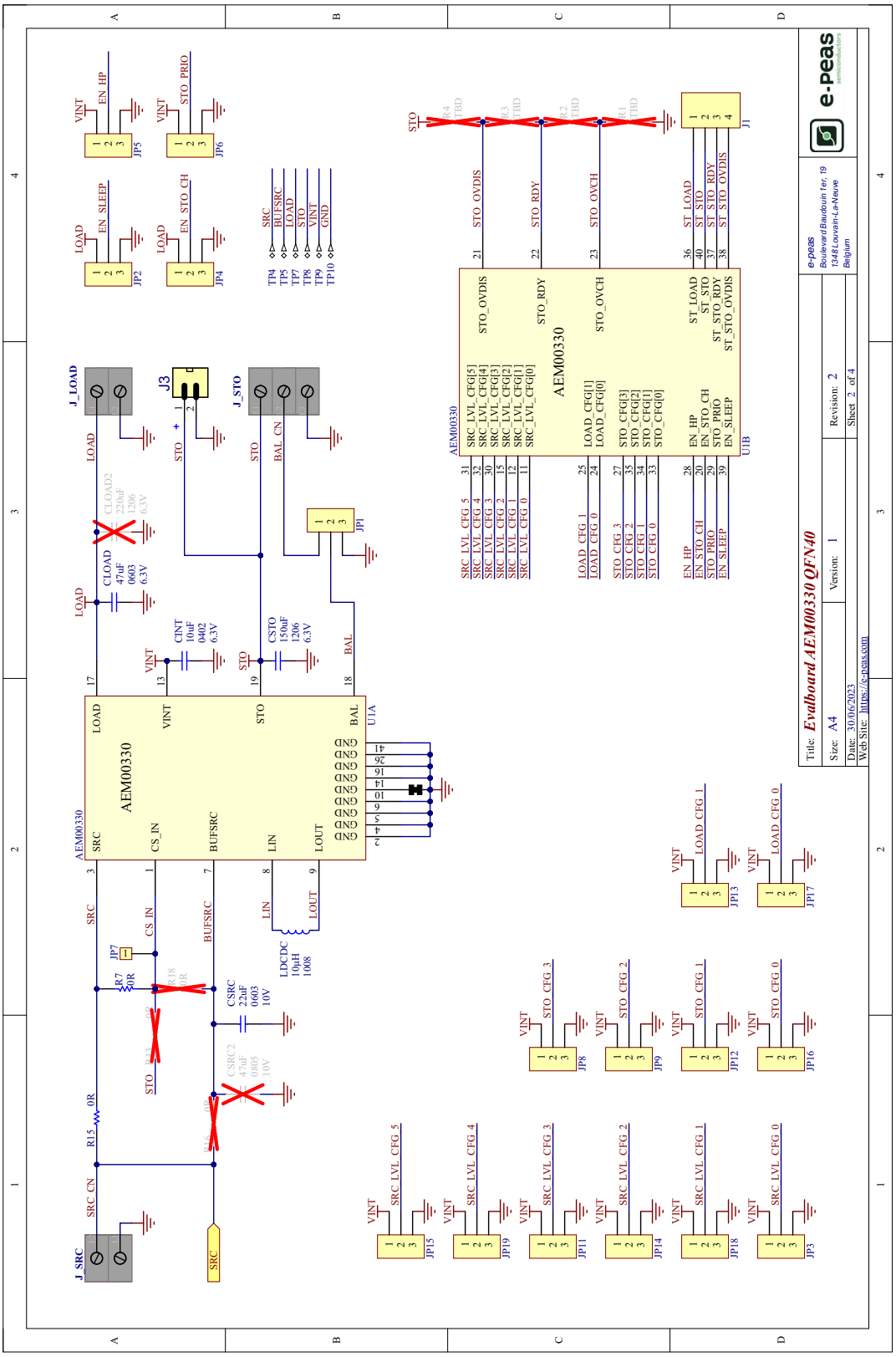

Figure 2: Schematic Part 1

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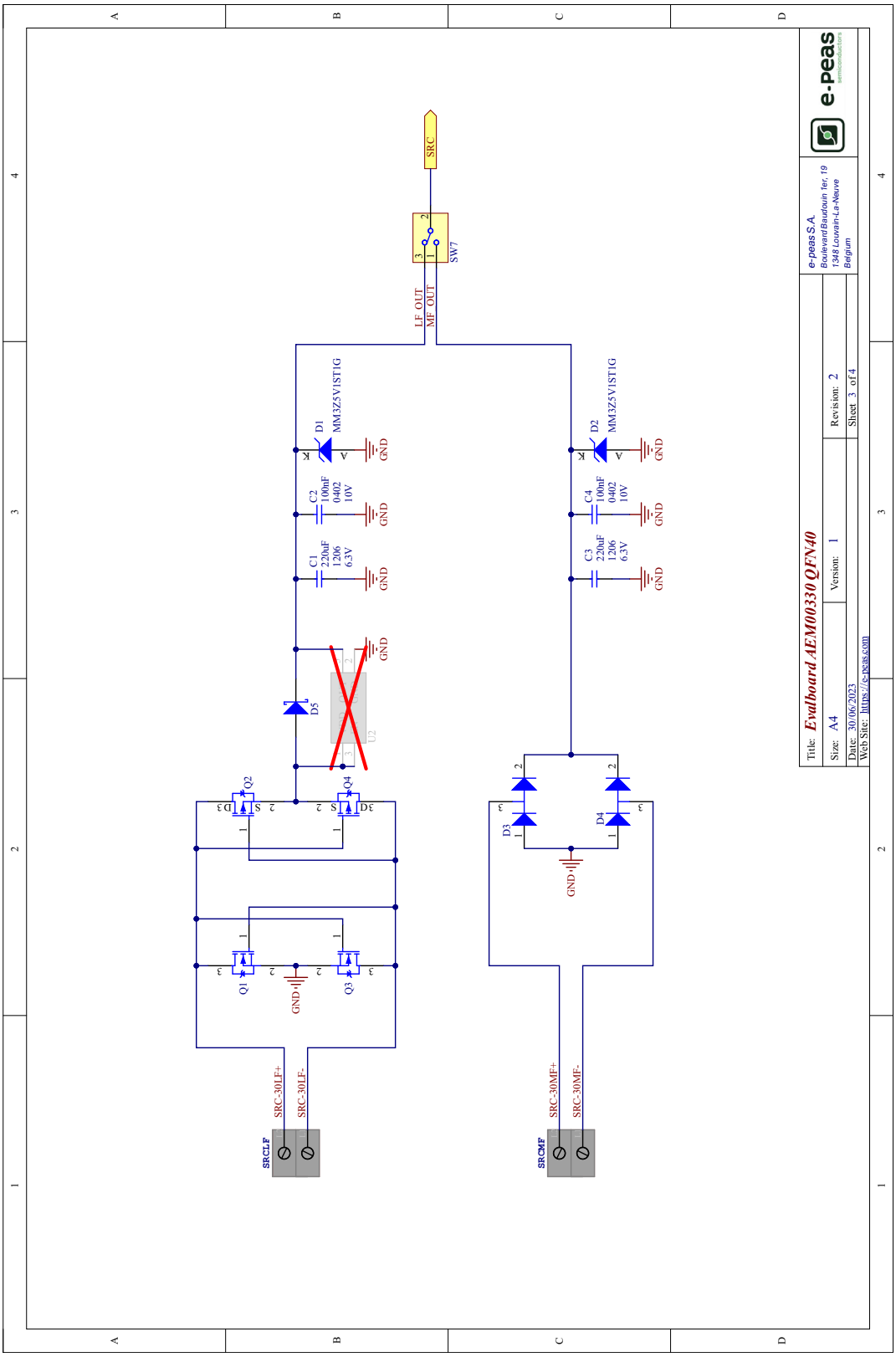

Figure 3: Schematic Part 2

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5. Revision History

EVK Version	User Guide Revision	Date	Description
Up to 1.1	1.0	September, 2021	Creation of the document.
	1.1	November, 2022	Fixed some inconsistencies and updated images.
1.2	1.0	August, 2023	Images and schematics update to EVK v1.2.
1.2	1.1	December, 2023	- Updated Revision History table to separate EVK version and User Guide version. - Replaced 0/1 by L/H.
1.2	1.2	February, 2024	Removed references to LOAD_CFG[2] pin.

Table 5: Revision History

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