Compact Ultra-Efficient PMIC with Maximum Power Point Tracking for Single/Dual PV Cells

Features and Benefits

Cold start from 250 mV input voltage and 5 µW input power (typical)
- Fast start-up from source.

Maximum Power Point Tracking
- Matches various single/dual elements PV cells;
- Configurable MPPT ratios of 35, 50 and from 60 to 90% by 5% steps;
- Constant impedance matching (QFN package only);
- Configurable MPPT sensing timing and period;
- MPPT voltage operation range from 115 mV to 1.5 V.

Selectable overdischarge and overcharge protection
- Supports various types of rechargeable batteries (LiC, Li-ion, LiPo, super capacitor, Li-ceramic pouch, etc.).

Ultra-low power idle modes
- Stored energy is preserved when no source available.

Shipping and shelf mode
- Prevents energy drain from battery when no source available (KEEP_ALIVE pin);
- Disables storage element charging (DIS_STO_CH pin).

Configuration pins or I²C
- Easy setup;
- Basic settings at startup with configuration pins;
- Advanced configuration with I²C.

Average power monitoring
- Easy estimation of the harvested power.

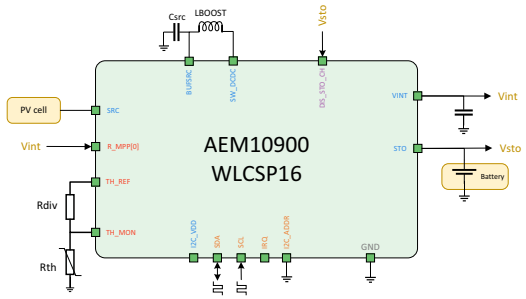
Integrated thermistor conditioning circuit
- Configurable battery thermal protection

WLCSP16-pin 2x2 mm or QFN 28-pin 4x4mm
- Small PCB footprint and low cost.

Only three passive components required
- Low BOM cost.

Applications

Wearable Electronics	Keyboards
Remote Control Units	Electronic Shelf Labels
Smart Buildings	Indoor Sensors



Description

The AEM10900 is a fully integrated and compact battery charger circuit that extracts DC power from a harvester to store energy in a rechargeable battery. This compact and ultra-efficient battery charger allows to extend battery lifetime and eliminates the primary energy storage in a large range of wireless applications, such as wearable electronics, ESL, keyboards, RCU and smart buildings.

Thanks to a Maximum Power Point Tracking and a ultra-low power boost converter, the AEM10900 harvests the maximum available power from a source to charge a storage element, such as a Li-ion battery or a LiC. The boost converter operates with input voltages ranging from 115 mV to 1.5 V, making AEM10900 ideal for single or dual element PV cell.

With its unique cold-start circuit, it can start operating with an input voltage as low as 250 mV and an input power of only 5 µW. The output voltages are in a range of 2.8 V to 4.8 V.

The configurable protection levels determine the storage element voltage protection thresholds to avoid overcharging and overdischarging the storage element and thus damaging it. No external components are required to set those levels.

Thermal monitoring protects the storage element. Average power monitoring system (APM) allows the application circuit to get a measure of harvested energy.

Thanks to the Keep-alive feature, the AEM10900 internal circuit can stay powered by the storage element even in absence of an harvesting source. This prevents to cold-start when harvesting energy is back. When Keep-alive is disabled and no harvesting source is present, the AEM10900 turns off, preserving the energy of the storage element.

A shelf-mode can be obtained by disabling the Keep-alive feature, preventing the battery to be drained during device storage. Furthermore, disabling the Keep-alive feature creates a shipping mode by preventing battery charging.

AEM10900 enables small size and low cost implementation for single/dual element PV or pulsed sources versus other DCDC based solutions.

Device Information

Part Number	Package	Body size
10AEM10900D0000	WLCSP16-pin	2x2mm
10AEM10900C0000	QFN 28-pin	4x4mm

Evaluation Board

Part number
2AAEM10900C001

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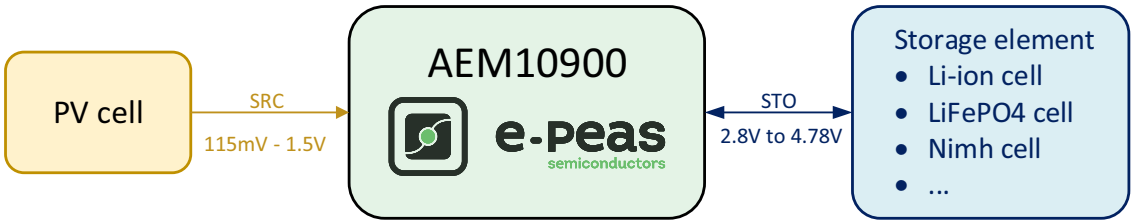


Figure 1: Simplified schematic view

1. Introduction

The AEM10900 is a full-featured energy efficient battery charger able to charge a storage element (connected to STO) from an energy source (connected to SRC).

The core of the AEM10900 is a regulated switching converter (boost) with high-power conversion efficiency.

At first start-up, as soon as a required cold start voltage of 250 mV and a sparse amount of power of at least 5 µW is available at the source (KEEP_ALIVE set to high), the AEM10900 coldstarts. After the cold start, the AEM extracts the power available from the source if the input voltage is higher than 115 mV.

The AEM10900 can be fully configured through the I²C interface or partially by configuration pins (depending on the package). I²C configuration is not mandatory, as the default configuration is made to fit the most common needs, along with the configuration pins for the most common settings (depending on the package).

Through I²C communication or through the configuration pins, the user can select a specific operating mode from a variety of modes that cover most application requirements without any dedicated external component. The battery protection thresholds (V_{OVCH} and V_{OVDIS}) have a default value. They can also be configured in 60 mV steps using the I²C bus or the configuration pins STO_CFG[2:0] (QFN28 package only).

The Maximum Power Point (MPP) ratio is configurable by the configuration pins (R_MPP[2:0] on QFN28 package, R_MPP[0] on WLCSP16) or by the I²C interface. It ensures an optimum biasing of the harvester to maximize power extraction. The user can select a specific MPP ratio from two values (WLCSP16 package) or from eight values (QFN28 package), set by the configuration pins. With the I²C interface, the user can select a ratio amongst 9 different values.

Depending on the harvester, it is possible to adapt the timing between two MPP evaluations and the open circuit duration with the I²C communication but also with the configuration pins T_MPP[1:0] for the QFN28 version. There is a range of eight timing pairs.

AEM10900 features an optional temperature protection. It is set through the I²C interface and allows to define a temperature range so that, when the ambient temperature is outside that range, battery charging is disabled. One additional resistor and one additional thermistor are needed for this feature.

The KEEP_ALIVE functionality sets the source to supply the AEM10900 internal circuitry VINT, which can be supplied either from the harvester connected on SRC or from the battery connected to STO. When supplied by SRC, the AEM10900 internal circuitry is running as long as enough energy is available on SRC. If no energy is available on SRC, the internal voltage drops until reset voltage and the AEM needs to go through a cold start before being able to charge the battery again. This is useful for applications with long periods without energy on SRC and when the I²C is not used. With this setting there is no quiescent current taken from the battery to supply the AEM10900 and the power balance is always positive. When supplied by STO, the circuit stays in SUPPLY STATE or SLEEP STATE as long as the battery connected to STO is above the over-discharge threshold. It prevents loosing the I²C configuration when energy harvesting is not occurring while minimizing the leakage on the battery.

The AEM10900 prevents the charging of the battery on STO, when the environment conditions do not allow to charge it safely thanks to the thermal monitoring.

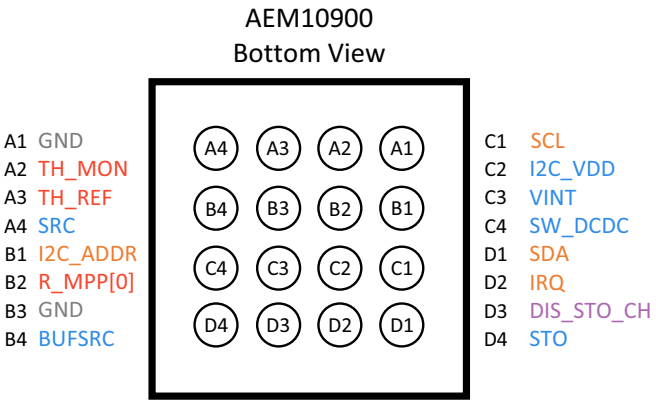


Figure 2: Pinout diagram WLCSP16

Name	Pin Number	Function
Power Pins		
SRC	A4	Connection to the harvested energy source.
BUFSRC	B4	Connection to an external capacitor buffering the boost converter input.
SWDCDC	C4	Switching node of the boost converter.
VINT	C3	Internal voltage supply.
I2C_VDD	C2	Connection to I²C supply voltage. Connect to GND if not used.
STO	D4	Connection to the energy storage element (battery). Cannot be left floating, voltage must always be above 2.8 V.
I²C Pins		
SDA	D1	Bidirectional data line. Connect to I2C_VDD if not used.
SCL	C1	Unidirectional serial clock for I²C. Connect to I2C_VDD if not used.
IRQ	D2	Output Interrupt request. Left floating if not used.
I2C_ADDR	B1	Configuration bit for I²C address. Read as high if left floating. - If set high, the address is 0x41. - If set low, the address is 0x40.
Configuration Pins		
TH_REF	A3	Reference voltage for thermal monitoring. Leave floating if not used.
TH_MON	A2	Pin for temperature monitoring. Connect to VINT is not used.
R_MPP[0]	B2	Used for the configuration of the MPP ratio. Read as high if left floating.
Control pins		
DIS_STO_CH	D3	When asserted, the AEM stops charging the battery. Read as low if left floating.
Other Pins		
GND	A1, B3	Ground connection, both terminals should be strongly tied to the PCB ground plane.

Table 1: Pins description WLCSP16

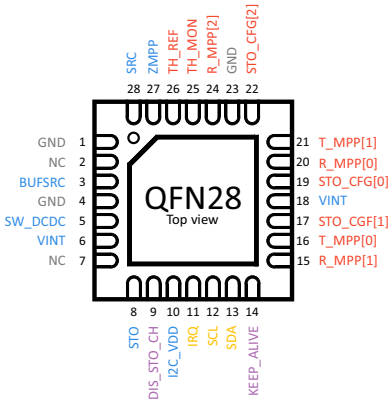


Figure 3: Pinout diagram QFN28

NAME	PIN NUMBER	Function
Power Pins		
SRC	28	Connection to the harvested energy source.
BUFSRC	3	Connection to an external capacitor buffering the boost converter input.
SWDCDC	5	Switching node of the boost converter.
VINT	6, 18	Internal voltage supply.
STO	8	Connection to the energy storage element (rechargeable battery). Cannot be left floating, voltage must always be above 2.8 V.
I2C_VDD	10	Connection to supply I²C interface. - Connect to a 1.5 V to 2.2 V power supply if I²C is used. - Connect to GND if I²C is not used.
ZMPP	27	Connection for R_{ZMPP} (Must be left floating when not used)
I²C Pins		
SDA	13	Bidirectional data line. Connect to I2C_VDD if not used.
SCL	12	Unidirectional serial clock for I²C. Connect to I2C_VDD if not used.
IRQ	11	Output Interrupt request. Leave floating if not used.
Configuration Pins		
STO_CFG[0]	19	Used for the configuration of the threshold voltages for the energy storage element. Read as high if left floating.
STO_CFG[1]	17	
STO_CFG[2]	22	
T_MPP[0]	16	Used for the configuration of the MPP timings. Read as high if left floating.
T_MPP[1]	21	
R_MPP[0]	20	Used for the configuration of the MPP ratio. Read as high if left floating.
R_MPP[1]	15	
R_MPP[2]	24	
TH_REF	26	Reference voltage for thermal monitoring. Leave floating if not used.
TH_MON	25	Pin for temperature monitoring. Connect to VINT if not used.
Control Pins		
DIS_STO_CH	9	When high, the AEM stops charging the battery. Read as low if left floating.
KEEP_ALIVE	14	When high, the internal circuitry is supplied from STO. When low, the internal circuitry is supplied from SRC.
Other pins		
GND	1, 4, 23, back plane	Ground connection, each terminal should be strongly tied to the PCB ground plane.
NC	2, 7	Not connected pins, leave floating.

Table 2: Pins description QFN28

2. Absolute Maximum Ratings

Parameter	Value
Voltage on SRC	2.0 V
Voltage on STO	5.5 V
Voltage in I2C_VDD	2.2V
Operating junction temperature	-40°C to 125°C
ESD HBM voltage	TBD
ESD CDM voltage	TBD

Table 3: Absolute maximum ratings

3. Thermal Resistance

Package	θJA	θJC	Unit
WLCSP16	TBD	TBD	°C/W
QFN28	TBD	TBD	°C/W

Table 4: Thermal data

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

4. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$P_{SRC,CS}$	Minimum source power required for cold start	During cold start KEEP_ALIVE = VINT		5		µW
		During cold start KEEP_ALIVE = GND		14		µW
$V_{SRC,CS}$	Minimum source voltage required for cold start			0.25		V
V_{MPP}	Target regulation voltage on SRC when extracting power.		0.12		1.50	V
V_{OC}	Open-circuit voltage of the source				2.0	V
Timing						
T_{VOC}	Open-circuit duration for the MPP evaluations		See Table 8			ms
T_{MPPT}	Time between two MPP evaluations					s
Storage Element						
V_{STO}	Voltage on the storage element		2.81		4.78	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging		3	See section 8.4	4.78	V
V_{OVDIS}	Minimum voltage accepted on the storage element before stopping to supply VINT if Keep-alive is enabled.		2.81		4.05	V
Internal supply & Quiescent Current						
V_{INT}	Internal voltage supply			2.2		V
$I_{QSUPPLY}$	Quiescent current on VINT in SUPPLY STATE	V_{STO} = 3.7 V		300		nA
I_{QSLEEP}	Quiescent current on VINT in SLEEP STATE	V_{STO} = 3.7 V		150		nA
I_{QSTO}	Quiescent current on STO when Keep-alive functionality is disabled			1		nA
$T_{RESET,SLEEP}$	Delay before reset when no energy on SRC and Keep-alive functionality disabled, or if Keep-alive is enabled but the battery voltage dropped below V_{OVDIS}	C_{INT} = 3.3 µF (leakage neglected), AEM in SLEEP STATE, no I²C communication		2.2		s
$T_{RESET,SUPPLY}$		C_{INT} = 3.3 µF (leakage neglected), AEM in SUPPLY STATE, no I²C communication		1.1		s

Table 5: Electrical characteristics

5. Recommended Operation Conditions

Symbol	Parameter		Min	Typ	Max	Unit
External Components						
L_{DCDC}	Inductor of the boost converter		3.3	6.8		µH
C_{SRC}	Capacitor decoupling the BUFSRC terminal		10			µF
C_{INT}	Capacitor decoupling the internal voltage		3.3			µF
C_{STO}	Optional - capacitor decoupling the STO terminal[1]		22			µF
R_{ZMPP}	Optional - Resistor for the ZMPPT configuration (see Section 8.3)		33		1M	Ohm
R_{DIV}	Optional - pull-up resistor for the thermal monitoring		5k	22k	33k	Ohm
R_{TH}	Optional - thermistor for the thermal monitoring	R0		10k		Ohm
		Beta		3380		K
R_{SCL} / R_{SDA}	Optional - pull-up resistors for the I²C interface			1k		Ohm
Logic input Pins						
R_MPP[2:0]	Configuration pins for the MPP ratio	Logic high	Connect to VINT			
		Logic low	Connect to GND			
T_MPP[1:0]	Configuration pins for the MPP timings	Logic high	Connect to VINT			
		Logic low	Connect to GND			
STO_CFG[2:0]	Configuration pins for the storage element thresholds	Logic high	Connect to VINT			
		Logic low	Connect to GND			
KEEP_ALIVE	Configuration for the “Keep alive” functionality	Logic high	Connect to VINT			
		Logic low	Connect to GND			
DIS_STO_CH	Configuration for disabling the charging of the battery	Logic high	Connect to STO			
		Logic low	Connect to GND			
I²C Interface Pins						
I2C_VDD	I²C interface supply pin		1.5		2.2	V
SCL / SDA	I²C interface communication pins		Pull-up to I2C_VDD with resistors			

Table 6: Recommended operating conditions

1.Decoupling capacitor is recommended to ensure optimal efficiency of the DCDC converter when using a storage element that has significant internal resistance (ESR). It is also recomended when measuring the AEM10900 efficiency with laboratory equipment such as source measurement units (SMU).

6. Functional Block Diagram

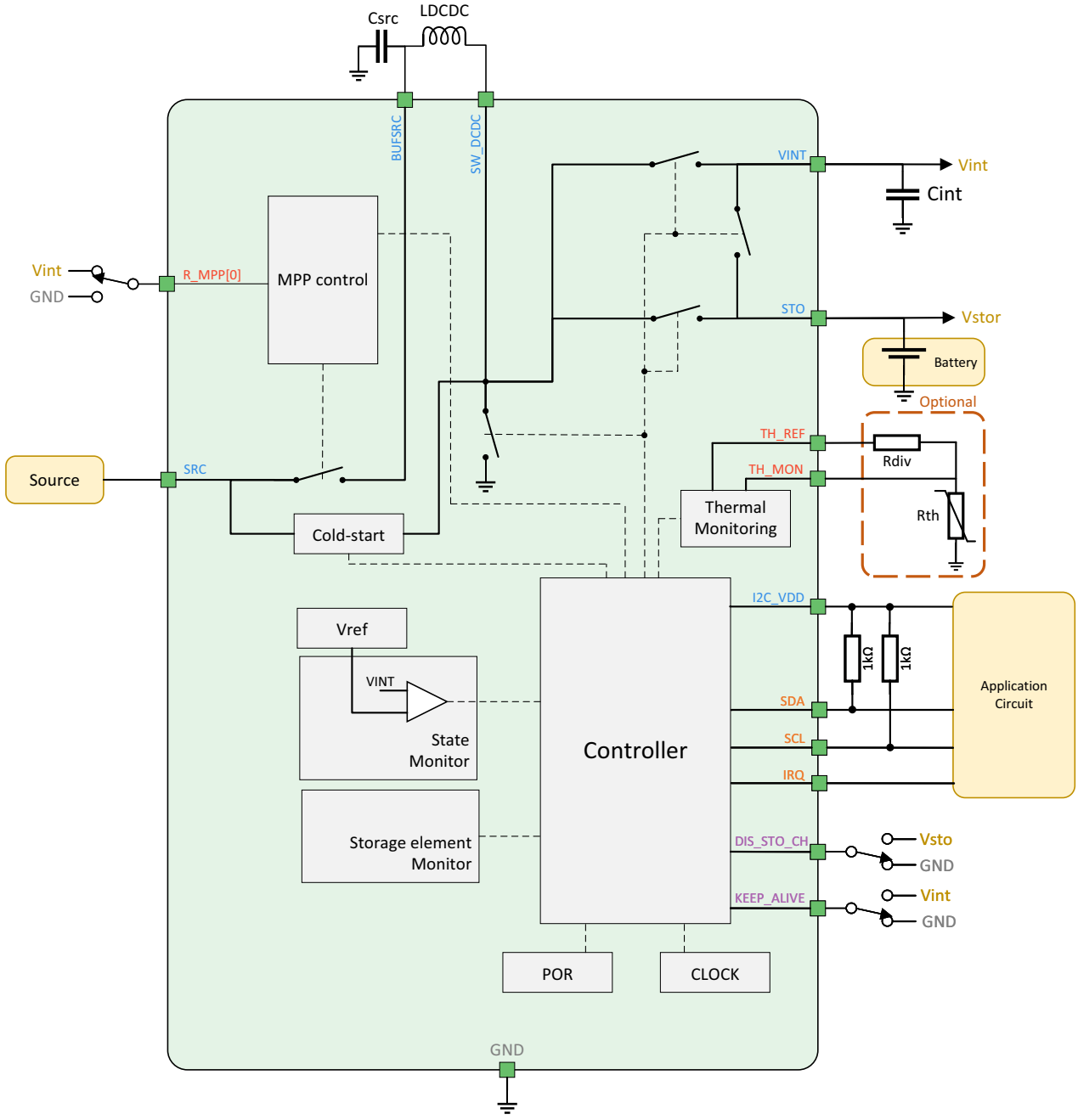


Figure 4: Functional block diagram (WLCSP16 package)

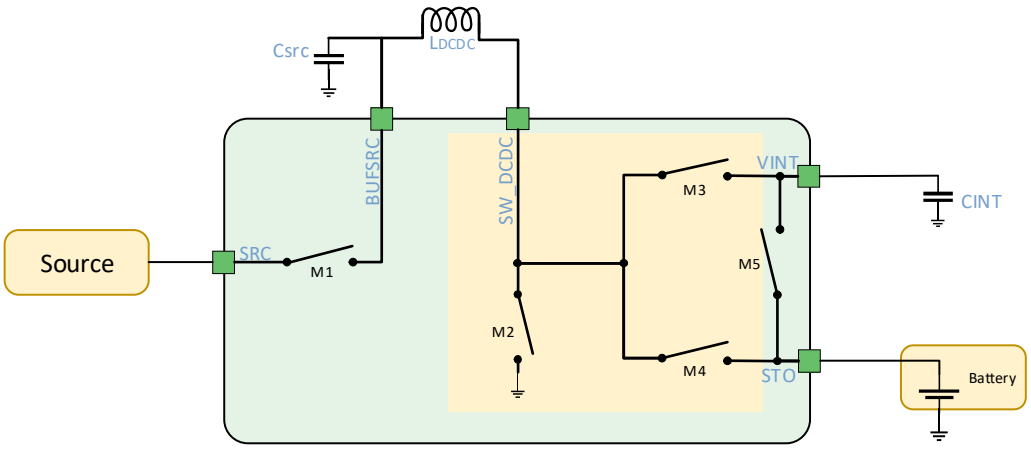


Figure 5: Simplified schematic view of the AEM10900

7. Theory of Operation

7.1. Boost Converter

The boost (step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.81 V to 4.78 V, according to the system configuration. The switching transistors of the boost converter are M2, M3 and M4. The reactive power component of this converter is the external inductor L_{DCDC}.

Periodically, the MPP control circuit disconnects SRC and BUFSRC pins (transistor M1) in order to measure the open-circuit voltage of the harvester and evaluate the input target voltage. BUFSRC is decoupled by the capacitor C_{SRC}, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the STO pin, which voltage is V_{STO}. This node is linked to the output of boost converter through transistor M4. When energy harvesting is occurring the boost converter charges the battery. M4 disconnects the storage element when V_{STO} reaches V_{OVCH}. If VINT drops below its regulation value and if Keep-alive functionality is disabled, the AEM switches its output by enabling M3 instead of M4 until VINT reaches its target plus a small hysteresis. If the Keep-alive functionality is enabled, VINT is instead supplied from STO by modulating the gate of M5. In this case M3 is never activated.

7.2. Maximum Power Point Tracking

The AEM10900 has a Maximum Power Point Tracking (MPPT) module, that relies on the fact that, for several models of harvesters (typ. solar cells), the ratio between the maximum power point voltage (V_{MPP}) and the open circuit voltage (V_{OC}) is constant for a wide range of harvesting conditions. For a solar cell, that means that V_{MPP} / V_{OC} is constant for any lighting conditions, even though both voltages increase when luminosity increase.

The MPP ratio (V_{MPP} / V_{OC}) differs from one harvester model to the other. User must set the MPP ratio to match the specifications of the harvester model used and thus maximize power extraction. This ratio is set by the I²C interface or with the configuration pins R_MPP[2:0] according to table 7.

The MPPT module evaluates the open circuit voltage V_{OC} periodically to ensure optimal power extraction at any time. The sampling period T_{MPPT} and sampling duration T_{VOC} of the evaluation of V_{OC} are set according to table 8 by configuring the RATIO field in the MPPTCFG register or with the configuration pins T_MPP[1:0]. Every T_{MPPT}, the MPPT stops extracting power from the source, waits during T_{VOC} for the source to rise to its open circuit voltage V_{OC}, and measures V_{OC}. The AEM10900 supports multiple V_{MPP} levels in the range from 0.12 V to 1.50 V. It offers a choice of up to nine values for the V_{MPP} / V_{OC} fraction.

The MPPT module is active during SUPPLY STATE, SENSE SRC STATE and SENSE STO STATE.

7.3. Thermal Monitoring

Thermal monitoring allows to protect the storage element. Enabling this functionality requires the use of a resistor (R_{DIV}) and a thermistor (R_{TH}). See figure 6 for external components connections. The TH_REF terminal allows a reference voltage to be applied to the resistive divider while TH_MON is the measuring point. The temperature evaluation is done periodically (typ. every 8 s) to spare power. Information for the thermal monitoring is described in section 8.8.3. Thermal monitoring is optional, if not used connect TH_MON to VINT and leave TH_REF floating.

Figure 6: TH_REF and TH_MON connections

7.4. Average Power Monitoring

The Average Power Monitoring (APM) allows to evaluate the energy transfer from SRC to STO. The APM is able to determine the transferred energy by counting the number of current pulses transferred to STO by the boost converter over a configurable time window, and thus evaluate the corresponding energy.

Two modes are available: Pulse Counter Mode and Power Meter Mode.

The APM behaviour is described in Figure 7:

- **Phase A**:
  - **Pulse Counter Mode**: APM counts the number of DCDC pulses happening during T_A
  - **Power Meter Mode**: APM integrates the energy transferred from SRC to STO during T_A
- **Phase B**: APM waits during $T_B = T_A$
- **IRQ**: a rising edge is triggered on the IRQ pin, if IRQEN.APMDONE field is set to 1 (see Section 8.8.8 and Section 8.8.10). A rising edge on IRQ along with the IRQFLAG.APMDONE field set to 1 indicates to the user that a new value is available and ready to be read in the APM Data Register (APMx, Section 8.8.12).

Refer to Section 8.8.7. for further details about how to set modes, how to convert registers value to Joule and how to set T_A.

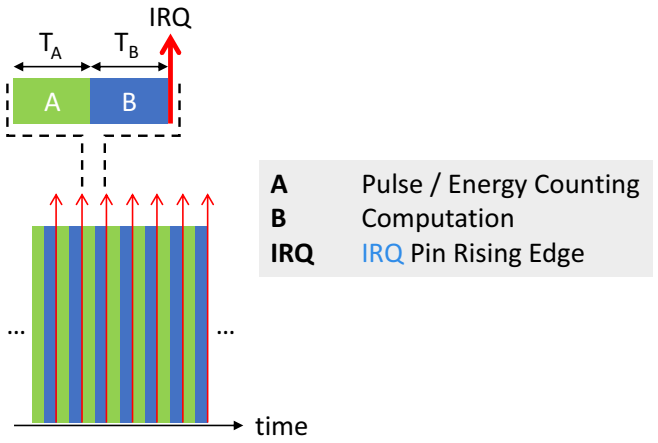


Figure 7: Average Power Monitoring description

7.5. Automatic High Power Mode

When the AEM detects that the energy available on SRC is high enough, the boost converter automatically switches to high-power mode.

Preventing the AEM to switch to high-power mode may allow to use an inductor with half peak current rating for L_{DCDC} (see Section 8.9.2). On the other hand, allowing the AEM to switch to high-power mode increases the maximum current that the AEM can harvest from SRC to STO.

Automatic high-power mode is enabled by default and can be disabled by setting the PWR.HPEN to 0 through the I²C interface.

7.6. Keep-alive

The internal circuitry connected to VINT can be supplied either by SRC through the boost converter (Keep-alive disabled), or by the battery STO (Keep-alive enabled).

When supplied from SRC, the AEM10900 switches to RESET STATE when the energy available on SRC is not sufficient. The advantage is that no energy is pulled from the battery when the AEM10900 is not harvesting energy from SRC (I_{QSTO} in Table 5). The drawback is that the AEM has to coldstart after every period without enough energy on SRC.

When the Keep-alive mode is enabled, VINT is regulated as long as enough energy is available from the battery on STO. This function is useful when the energy available on SRC is not stable, and allows to maintain I²C registers configuration. Referring to Table 5, the quiescent current is then $I_{QSUPPLY}$ or I_{QSLEEP}, depending on whether the AEM10900 is in SUPPLY STATE or in SLEEP STATE.

7.7. IRQ Pin

The IRQ pin allows user to get an interrupt triggered by various AEM10900 events (rising edge on IRQ pin). At startup, the only interrupt that is enabled is I2CRDY, allowing user to know when the AEM10900 has finished to coldstart and thus, is out from RESET STATE. Other interrupts can be enabled by writing the IRQEN register (Section 8.8.8). When the IRQ pin shows a rising edge, the interrupt source can be determined by reading the IRQFLG register (Section 8.8.10).

7.8. State description

7.8.1. Reset State

In RESET STATE all nodes are deeply discharged and there is no available energy to be harvested. The AEM stays in this state until the source connected to SRC meets the cold start requirements long enough to make VINT rise up to 2.2 V. Cold start requirements depend on whether the Keep-alive feature is enabled or not:

- KEEP_ALIVE = 1:
  - V_{SRC} ≥ 250 mV
  - $P_{SRC,CS}$ ≥ 5 µW
- KEEP_ALIVE = 0:
  - V_{SRC} ≥ 250 mV
  - $P_{SRC,CS}$ ≥ 14 µW

When VINT has reached 2.2 V, the AEM10900 reads the configuration pins and switches to SENSE SRC STATE.

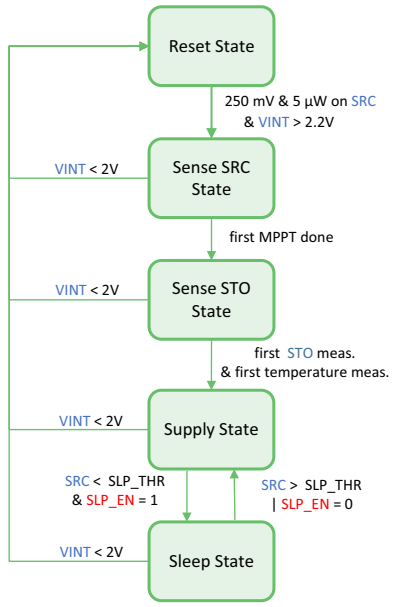


Figure 8: Diagram of the AEM10900 state

7.8.2. Sense SRC State

In SENSE SRC STATE, the AEM10900 does a first MPPT to evaluate the power available at SRC. The MPPT is described in Section 7.2..

The next step is therefore to determine whether the battery can be charged. This mode is called SENSE STO STATE.

7.8.3. Sense STO State

In SENSE STO STATE the AEM10900 does the following measurements:

- Battery voltage on STO;
- Temperature through pins TH_MON and TH_REF (see Section 7.3. and 8.8.3.).

The AEM10900 then switches to SUPPLY STATE.

7.8.4. Supply State

In SUPPLY STATE, the AEM transfers charges directly from SRC to STO while maintaining V_{INT}.

If V_{INT} drops and the energy available on SRC is not sufficient to make V_{INT} rise again, there are two possible behaviors, depending on the 'Keep Alive' feature:

- If 'Keep alive' is enabled, Vint is supplied by the battery through M5, so the AEM10900 stays in SUPPLY STATE while energy is available on the battery;
- If 'Keep alive' is disabled, the AEM internal circuitry will no longer be maintained and the AEM switches to RESET STATE.

7.8.5. Sleep State

Please note that the first condition for the AEM10900 to enter SLEEP STATE is to set the SLEEP.EN field in the SLEEP register 1, as shown on Figure 1.

In SLEEP STATE, the AEM power consumption is reduced, since the power available on the input is presumably low (V_{SRC} below the threshold voltage defined by the SLEEP.THRESH field). If the source voltage rises again above the threshold, or if the SLEEP.EN field is set to 0, the AEM10900 switches back to SUPPLY STATE. SLEEP STATE entering or exiting is triggered by the MPP acquisitions.

SLEEP STATE is enabled by default with a 105 mV threshold. It is not recommended to disable SLEEP STATE for standard uses of the AEM10900.

8. System Configuration

8.1. Configuration Pins and I²C

8.1.1. Configuration Pins

After a cold start, the AEM10900 reads the configuration pins. Those are then read periodically every 2 s, with the exception of the DIS_STO_CH pin that is read every 1 s. The configuration pins can be changed on-the-fly. The floating configuration pins are read as 1, except DIS_STO_CH which is read as 0.

8.1.2. Configuration by I²C

To configure the AEM10900 through the I²C interface after a cold start, user must wait for the IRQ pin to rise, showing that the AEM10900 is out of RESET STATE and is ready to communicate with I²C. Please note that the IRQ pin is always low during RESET STATE. See Section 8.8.10 for further informations about the IRQ pin.

Once the above procedure is done, user can then write to the desired registers and validate the configuration by setting the CTRL.UPDATE register field. All configuration pins are then ignored and all the configurations are set by the register values. All registers have a default value, that can be found in Table 10.

Registers are stored in a volatile memory, so their value is lost when VINT drops below the reset voltage (2 V), making the AEM10900 switch to RESET STATE. Thus, when using the I²C configuration, it is highly recommended to enable the Keep-alive functionality (see section 8.8.4.). If the Keep-alive functionality is disabled, register configuration is lost every time the energy available SRC is not sufficient to maintain V_{INT} above the reset voltage (2 V).

8.2. MPPT Configuration

Two parameters are necessary to configure the Maximum Power Point Tracking. The first parameter is the MPP tracking ratio, which is selected according to the characteristics of the input power source. This parameter is set on bits [3:0] of the MPPTCFG (0x01) register, or by the configuration pins for the QFN28 package. On the WLCSP16 package, only R_MPP[0] is available as a configuration pin.

The second parameter allows configuring the duration of the evaluation of V_{OC} and the time between two MPP evaluations. The configuration is set on bits [6:4] of the MPPTCFG (0x01) register, or by the configuration pins for the QFN28 package.

Configuration	Availability Through Pins			MPPT ratio
R_MPP[3:0]	I²C Interface	Configuration pins		Vmpp/Voc
		QFN28	WLCSP16	
0000	yes	yes	no	ZMPP
0001	yes	yes	no	90%
0010	yes	yes	no	65%
0011	yes	yes	no	60%
0100	yes	yes	no	85%
0101	yes	yes	no	75%
0110	yes	yes	yes	70%
0111	yes	yes	yes	80%
1000	yes	no	no	35%
1001	yes	no	no	50%

Table 7: Configuration of MPP ratio

Configuration	Availability Through Pins			MPP Timing	
T_MPP[2:0]	I²C Interface	Configuration pins		Sampling duration T_{VOC} [ms]	Sampling period T_{MPPT} [ms]
		QFN28	WLCSP16		
000	yes	no	no	2	64
001	yes	no	no	256	16384
010	yes	no	no	64	4096
011	yes	no	no	8	1024
100	yes	yes	no	4	256
101	yes	yes	no	2	128
110	yes	yes	no	4	512
111	yes	yes	yes	2	256

Table 8: Configuration of MPP timing

8.3. ZMPP Configuration

Instead of working at a ratio of the open-circuit voltage, the AEM10900 can regulate the input resistance of the boost converter so that it matches a constant resistance connected to the ZMPP pin (R_{ZMPP}). In this case, the AEM10900 regulates V_{SRC} at a voltage equal to the product of the ZMPP resistance and the current available at the SRC input.

8.4. Storage Element Thresholds Configuration

It is possible to set the voltage thresholds for which the storage element is considered to be discharged (V_{OVDIS}) and fully charged (V_{OVCH}).

V_{OVDIS} is configured on the VOVDIS (0x02) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$\text{THRESH} = \frac{V_{OVDIS} - 0.50625}{0.05625}$$

THRESH is the integer value to be written in the register. The minimum value is 2.8 V. If the register value corresponds to V_{OVDIS} < 2.8 V, the threshold voltage is forced to 2.8 V.

V_{OVCH} is configured on the VOVCH (0x03) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$\text{THRESH} = \frac{V_{OVCH} - 1.2375}{0.05625}$$

THRESH is the integer value to be written in the register. The minimum value is 3.0 V. If the register value corresponds to V_{OVCH} < 3.0 V, the threshold voltage is forced to 3.0 V.

On the QFN28 package, it is also possible to configure V_{OVDIS} and V_{OVCH} with configuration pins STO_CFG[2:0] as shown in table 9.

Configuration	**Availability Through Pins**			**Storage element threshold voltage**	
STO_CFG[2:0]	**I²C Interface**	**Configuration pins**		**V_{OVCH}**	**V_{OVDIS}**
		QFN28	**WLCSP16**		
000	yes	yes	no	4.50 V	3.30 V
001	yes	yes	no	4.00 V	2.80 V
010	yes	yes	no	3.63 V	2.80 V
011	yes	yes	no	3.90 V	2.80 V
100	yes	yes	no	3.90 V	3.50 V
101	yes	yes	no	3.90 V	3.01 V
110	yes	yes	no	4.35 V	3.01 V
111	yes	yes	yes	4.12 V	3.01 V

Table 9: Usage of STO_CFG[2:0]

8.5. Disable Storage Element Charging

Pulling up DIS_STO_CH to STO disables the charging of the storage element connected to STO.

Please note that, if the Keep-alive feature is enabled by pulling up KEEP_ALIVE, VINT is supplied by STO regardless of the setting of DIS_STO_CH. To make sure that the storage element is neither charged nor used to supply VINT, user must both tie DIS_STO_CH to STO and tie KEEP_ALIVE to GND.

8.6. I²C Serial Interface Protocol

The AEM10900 uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (SDA) and a serial clock line (SCL). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

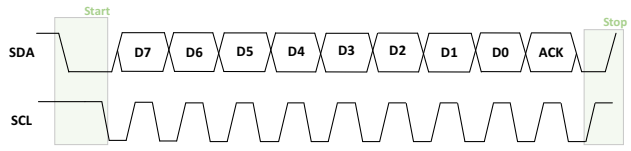


Figure 9: I²C transmission frame

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The AEM10900 is a slave that will receive configuration data or send the informations requested by the master.

The AEM10900 supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data are sent with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled-up (SDA and SCL are open drain outputs);
- Start bit (S): to initiates the transmission, the master switches the SDA line low while keeping SCL high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the SDA line from low to high while keeping SCL high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches SDA low;
- NACK: when the device receiving data keeps SDA high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x40 or 0x41 for the AEM10900, depending on the value of the I2C_ADDR pin. For packages where the I2C_ADDR pin is not present, the address is 0x41;
- Bit [0] is the communication mode: 1 for ‘read mode’ (used when the master reads informations from the slave) and 0 for ‘write mode’ (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

Here is the procedure for the master to write a slave register:

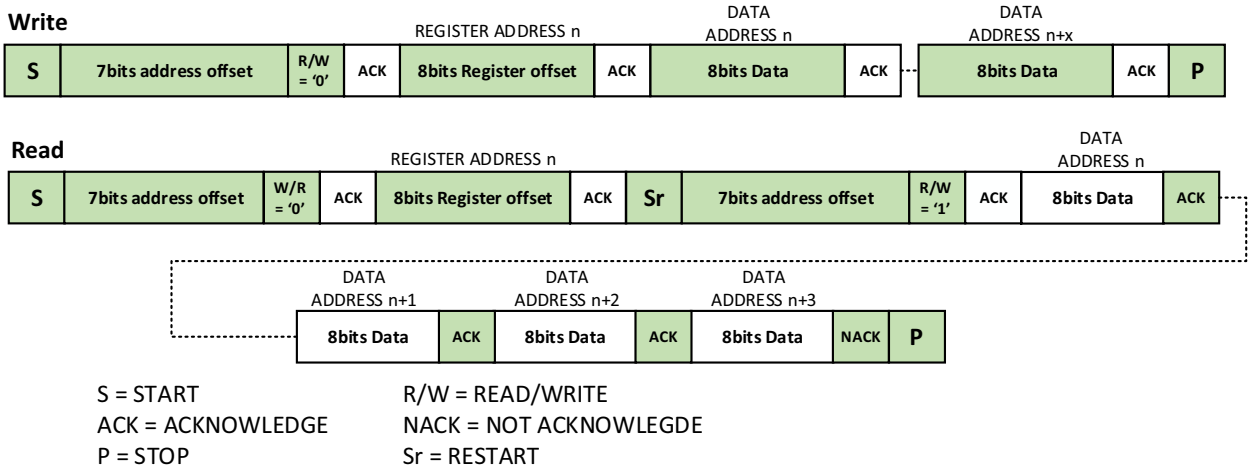
- Master sends the address of the slave in ‘write’ mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the TEMPCOLD register, the master sends the value 0x04;
- Slave sends an ACK;
- Master sends the data to write to the register;
- Slave sends an ACK;
- If the master wants to write register at the next address (TEMPHOT in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in ‘write’ mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the MPPTCFG register, the master sends the value 0x01;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in ‘read’ mode;
- Slave sends an ACK;
- Master provides the clock on SCL to allow the slave to shift the data of the read register on SDA;

- If the master wants to read register at the next address (STATUS.VOVDIS in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for writing several registers;
- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in the figure 10. Refer to Table 10 for all register addresses.



S = START
ACK = ACKNOWLEDGE
P = STOP
R/W = READ/WRITE
NACK = NOT ACKNOWLEGDE
Sr = RESTART

Figure 10: Read and write transmission

8.7. Registers Map

Address	Name	Bit	Field Name	Access	RESET	Description
0x00	VERSION	[3:0]	MINOR	R	-	Chip ID
		[7:4]	MAJOR	R	-	
0x01	MPPTCFG	[3:0]	RATIO	R/W	0x07 (85%)	MPPT ratio
		[6:4]	TIMING	R/W	0x07 (2ms/ 256ms)	MPPT timings
0x02	VOVDIS	[5:0]	THRESH	R/W	0x2D (3.05V)	Overdischarge level of the storage element
0x03	VOVCH	[5:0]	THRESH	R/W	0x33 (4.1V)	Overcharge level of the storage element
0x04	TEMPCOLD	[7:0]	THRESH	R/W	0x8F (0°C)	Cold temperature level
0x05	TEMPHOT	[7:0]	THRESH	R/W	0x2F (45°C)	Hot temperature level
0x06	PWR	[0:0]	KEEPALEN	R/W	0x01	Keepalive enable
		[1:1]	HPEN	R/W	0x01	High power mode enable
		[2:2]	TMONEN	R/W	0x01	Temperature monitoring enable
		[3:3]	STOCHDIS	R/W	0x00	Battery charging disable
0x07	SLEEP	[0:0]	EN	R/W	0x01	Sleep mode enable
		[3:1]	THRESH	R/W	0x00	Sleep threshold
0x08	STOMON	[2:0]	RATE	R/W	0x00	ADC rate
0x09	APM	[0:0]	EN	R/W	0x00	APM enable
		[1:1]	MODE	R/W	0x00	APM mode
		[3:2]	WINDOW	R/W	0x00	APM computation window
0x0A	IRQEN	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable
		[1:1]	VOVDIS	R/W	0x00	IRQ STO OVDIS enable
		[2:2]	VOVCH	R/W	0x00	IRQ STO OVCH enable
		[3:3]	SLPTHRESH	R/W	0x00	IRQ SRC LOW enable
		[4:4]	TEMP	R/W	0x00	IRQ temperature enable
		[5:5]	APMDONE	R/W	0x00	IRQ APM done enable
0x0B	CTRL	[0:0]	UPDATE	R/W	0x00	Load I²C registers configuration
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag
0x0C	IRQFLG	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag
		[1:1]	VOVDIS	R	0x00	IRQ STOR OVDIS flag
		[2:2]	VOVCH	R	0x00	IRQ STOR OVCH flag
		[3:3]	SLPTHRESH	R	0x00	IRQ SRC LOW flag
		[4:4]	TEMP	R	0x00	IRQ temperature flag
		[5:5]	APMDONE	R	0x00	IRQ APM done flag
0x0D	STATUS	[1:1]	VOVDIS	R	0x00	Status STO OVDIS
		[2:2]	VOVCH	R	0x00	Status STO OVCH
		[3:3]	SLPTHRESH	R	0x00	Status SRC LOW
		[4:4]	TEMP	R	0x00	Status temperature
		[6:6]	CHARGE	R	0x00	Status STO CH
0x0E	APM0	[7:0]	DATA	R	0x00	APM data 0
0x0F	APM1	[7:0]	DATA	R	0x00	APM data 1
0x10	APM2	[7:0]	DATA	R	0x00	APM data 2
0x11	TEMP	[7:0]	DATA	R	0x00	Temperature data
0x12	STO	[7:0]	DATA	R	0x00	Battery voltage
0x13	SRC	[7:0]	DATA	R	0x00	SRC ADC value

Table 10: Register summary

8.8. Registers Configurations

8.8.1. MPPT Register (MPPTCFG)

The MPPT register MPPTCFG (0x01) is composed of 2 parts. The first part is reserved for the MPP ratio. This parameter is set on bits [3:0] of the register. The second part allows configuring the duration of the evaluation of V_{OC} and the time between two MPP evaluations. The configuration is set on bits [6:4] of the register. All the information about the MPPT are available on section 7.2.

8.8.2. Storage Element Threshold Registers (VOVDIS, VOVCH)

The configuration of the storage element thresholds is done by setting two different registers through the I²C communication:

- The V_{OVDIS} threshold is configured in register VOVDIS (0x02);
- The V_{OVCH} threshold is configured in register VOVCH (0x03).

All the information about the storage element threshold voltage are available on section 8.4.

8.8.3. Temperature Register (TEMPCOLD, TEMPHOT)

The configuration of the temperature thresholds is done by setting two registers through I²C communication:

- The low temperature threshold is configured in register TEMPCOLD (0x04);
- The high temperature threshold is configured in register TEMPHOT (0x05).

The temperature protection uses a voltage divider consisting of the resistor R_{DIV} and the thermistor R_{TH}. Considering the specifications of the thermistor used, it is possible to determine the relationship between the temperature and the resistance of the thermistor. The following equation must therefore be applied to determine the value to be written to the register:

$$THRES = 256 \cdot \frac{R_{TH}}{R_{TH} + R_{DIV}}$$

The equation is the same for both the high and the low thresholds. THRESH is the value to be written to the registers, R_{TH} is the resistance of the thermistor at the threshold temperature and R_{DIV} is the resistance that creates a resistive divider with R_{TH}, as shown on figure 6. The AEM10900 determines if the ambient temperature is within the range previously set by measuring the voltage on pin TH_MON.

For example with a Murata NCP15XH103J03RC the default thresholds are 0°C and 45°C (see table 10), which matches the specifications of most Li-Ion batteries.

8.8.4. Power Register (PWR)

The PWR (0x06) register is dedicated to the power settings of the AEM10900 and is made of 4 bits:

PWR Register (0x06)			
Bit [3]	Bit [2]	Bit [1]	Bit [0]
STOCHDIS	TMONEN	HPEN	KEEPALEN
0	1	1	1

Table 11: PWR Register

Bit [3]: Battery charging disable (PWR.STOCHDIS).

This register is allowed in read and write mode.

Setting this bit to 0 allows the charging of the battery. Setting this bit to 1 disables it.

Bit [2]: Temperature monitoring enable (PWR.TMONEN).

The temperature monitoring enable bit enables the monitoring of the ambient temperature.

Setting this bit to 1 enables the temperature monitoring. Setting this bit to 0 disables it.

Bit [1]: High-power mode enable (PWR.HPEN).

Setting this bit to 1 allows the AEM to automatically enter high-power mode if needed, allowing for more power to be harvested from SRC (see section 7.5.).

Setting this bit to 0 disables automatic high-power mode.

Bit [0]: Keep alive enable (PWR.KEEPALEN).

This field defines the energy source from which the AEM10900 supplies VINT (internal circuitry).

When PWR.KEEPALEN is set to 0, VINT is supplied by SRC through the boost converter. When PWR.KEEPALEN field is set to 0, VINT is supplied by STO. Refer to section 7.6. for more informations.

NOTE: disabling the Keep alive feature is not recommended when configuring the AEM10900 with I²C registers, see Section 7.6.

8.8.5. Sleep Register (SLEEP)

The Sleep register SLEEP (0x07) enables the sleep mode and sets the conditions for entering the sleep mode.

SLEEP Register (0x07)			
Bit [3]	Bit [2]	Bit [1]	Bit [0]
THRESH			EN
0	0	0	1

Table 12: SLP register

Bit [3:1]: Sleep threshold (SLEEP.THRESH)

This field sets the voltage threshold below which the AEM10900 enters SLEEP STATE. Table 13 shows the available settings.

For example, if the sleep threshold is set to 010, the AEM will go into SLEEP STATE if the source voltage drops below 0.255V at the MPP ratio (V_{MPP}).

SLEEP.THRESH	
Configuration	Sleep threshold
000	0.105 V
001	0.202 V
010	0.255 V
011	0.300 V
100	0.360 V
101	0.405 V
110	0.510 V
111	0.600 V

Table 13: Configuration of the sleep threshold

Bit [0]: Sleep mode enable (SLEEP.EN)

This field enables SLEEP STATE when set to 1. When set to 0, the AEM10900 will never switch to SLEEP STATE. The sleep mode threshold is set to 112 mV.

8.8.6. Storage Element Acquisition Rate Register (STOMON)

This field (STOMON, 0x08) configures the acquisition rate of the ADC that measures STO voltage. Depending on the application, the source and the storage element, the user might want to increase the frequency of the acquisitions of the battery voltage, so that the acquisition rate is significantly faster than the expected voltage variation on the battery. Increasing this frequency increases the energy consumption of the AEM10900.

STOMON Register (0x08)		
Configuration	Sampling rate	Additional consumption on storage element (typ.)
000	Every 1.024 s	0.4 nA
001	Every 512 ms	0.8 nA
010	Every 256 ms	1.6 nA
011	Every 128 ms	3.2 nA
100	Every 64 ms	6.4 nA

Table 14: Acquisition rates for STO ADC

8.8.7. Average Power Monitoring Control Register (APM)

Average Power Monitoring (APM; register address 0x09) allows for estimating the energy transferred from the source to the battery over a certain period of time.

APM Register (0x09)			
Bit [3]	Bit [2]	Bit [1]	Bit [0]
WINDOW		MODE	EN
0	0	0	0

Table 15: APM register

Bit [3:2]: APM computation window (APM.WINDOW)

This field is used to select the APM computation window (noted T_A in Section 7.4). The energy transferred is integrated over this configurable time window.

APM.WINDOW		
Configuration	Computation window	APMx registers refresh rate
00	128 ms	256 ms
01	64 ms	128 ms
10	32 ms	64 ms

Table 16: Configuration of APM computation windows

Please note that, as described in Section 7.4, measurement period is twice the computation window, meaning that a new measurement is available every 2 x T_A.

The APM computation window is automatically managed by the AEM10900.

For users that would like to set the computation window manually: the MPP period must be at least twice longer than the APM computation window. If the user sets a value that does not comply with the previous condition, the AEM10900 will automatically change it to the largest compliant value.

Bit [1]: APM mode (APM.MODE)

The APM implements two modes:

- **Power meter mode**: the number of pulses during a period is multiplied by a value to obtain the energy that has been transferred taking into account the efficiency of the AEM10900. This mode is enabled by setting the APM mode bit to 1.
- **Pulse counter mode**: the AEM10900 counts the number of current pulses drawn by the boost converter. This mode is enabled by setting the APM mode bit to 0;

Bit [0]: APM enable (APM.EN)

This field enables the APM feature. When the APM.EN field bit is set to 1, it is enabled. If APM.EN field is set to 0, the feature is disabled.

8.8.8. IRQ Enable Register (IRQEN)

For some applications, it is interesting to have an interruption flag triggered by specific conditions on the IRQ pin. This register (IRQEN, 0x0A) enables those interrupts.

IRQEN Register (0x0A)					
Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
APMDONE	TEMP	SLPTHRESH	VOVCH	VOVDIS	I2CRDY
0	0	0	0	0	1

Table 17: IRQEN register

Bit [5]: IRQ APM done enable (IRQEN.APMDONE)

This bit enables the generation of an interrupt when new APM data is available.

When set to 0, the interrupt is disabled. When set to 1, the interrupt is enabled.

Bit [4]: IRQ temperature enable (IRQEN.TEMP)

This bit enables the generation of an interrupt when the temperature crosses the minimum or maximum temperature allowed to charge the battery (see section 8.6.3.).

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [3]: IRQ source low enable (IRQEN.SLPTHRESH)

This bit enables the generation of an interrupt when the AEM10900 sleep mode crosses the sleep mode threshold, which is set in the SLEEP register .

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [2]: IRQ storage over-charge enable (IRQEN.VOVCH)

This bit enables the generation of an interrupt when the battery voltage crosses the V_{OVCH} threshold.

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [1]: IRQ storage over-discharge enable (IRQEN.VOVDIS)

This bit enables the generation of an interrupt when the storage element voltage crosses the V_{OVDIS} threshold.

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [0]: IRQ serial interface ready enable (IRQEN.I2CRDY)

This interrupt is activated by default.

This bit enables the generation of an interrupt when the AEM10900 has coldstarted and is ready to communicate through I²C.

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

8.8.9. Control Register (CTRL)

The CTRL (0x0B) register is used to load the configuration done through the I²C interface. It includes two fields.

CTRL Register (0x0B)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
					SYNCBUSY		UPDATE
0	0	0	0	0	0	0	0

Table 18: CTRL register

Bit [2]: Synchronization busy flag (CTRL.SYNCBUSY)

This field indicates whether the synchronization from the I²C registers to the system registers is ongoing or not. After CTRL.UPDATE is set to 1, CTRL.SYNCBUSY is set while the registers written by I²C communication are being copied to the controller registers. CTRL.SYNCBUSY is reset to 0 when the copy is done and both I²C registers and controller registers are synchronized.

Bit [0]: Load configuration (CTRL.UPDATE)

This field is used to load all the I²C registers to the system registers and thus controls which configuration is active between the configuration pins and I²C. If the field is set to 0, the configuration pins will be used to configure the AEM10900. If it is set to 1, the configurations performed through I²C communications in the registers are loaded.

8.8.10. IRQ Flag Register (IRQFLG)

The IRQFLG (0x0C) register contains all interrupt flags, corresponding to those enabled in the IRQEN register.

IRQFLG Register (0x0C)					
Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
APMDONE	TEMP	SLPTHRESH	VOVCH	VOVDIS	I2CRDY
0	0	0	0	0	0

Table 19: IRQFLG register

Bit [5]: IRQ APM done Flag (IRQFLG.APMDONE)

This interrupt flag is set to 1 when a new APM data is available, if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption has not triggered.

Bit [4]: IRQ temperature Flag (IRQFLG.TEMP)

This interrupt flag is set to 1 when the temperature crosses the minimum or maximum temperature (selected through the TEMPCOLD and TEMPHOT registers), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption has not triggered.

Bit [3]: IRQ source low Flag (IRQFLG.SLPTHRESH)

This interrupt flag is set to 1 when the source crosses the sleep voltage (selected through the SLEEP register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption has not triggered.

Bit [2]: IRQ storage over-charge Flag (IRQFLG.VOVCH)

This interrupt flag is set to 1 when the battery crosses the overcharge voltage (selected through the VOVCH register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption has not triggered.

Bit [1]: IRQ storage over-discharge Flag (IRQFLG.VOVDIS)

This interrupt flag is set to 1 when the battery crosses the overdischarge voltage (selected through the VOVDIS register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption has not triggered.

Bit [0]: IRQ serial interface ready Flag (IRQFLG.I2CRDY)

This interrupt flag is set to 1 when the AEM10900 has coldstarted and is ready to communicate through I²C (the corresponding interrupt source is enabled by default). If this bit is 0, this interruption has not triggered.

8.8.11. Status Register (STATUS)

The STATUS (0x0D) register contains informations about the status of the AEM10900.

STATUS Register (0x0D)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
	CHARGE		TEMP	SLPTHRESH	VOVCH	VOVDIS	
0	0	0	0	0	0	0	0

Table 20: CTRL register

Bit [6]: Status STOR CH (STATUS.CHARGE)

This status indicates whether the AEM is currently charging the battery or not. If this bit is set to 0, the storage element charging is disabled. If it is set to 1, the storage element charging is enabled.

Bit [4]: Temperature Status (STATUS.TEMP)

This bit is set to 1 if the ambient temperature is outside the range defined by the TEMPCOLD and TEMPHOT registers. It is set to 0 is the temperature is within this range.

Bit [3]: Status SRC LOW (STATUS.SLPTHRESH)

This status indicates whether the source voltage is higher or lower than the sleep level threshold. If the source voltage is higher than the sleep level then the field is set to 0, else the field is set to 1.

Bit [2]: Status STOR OVCH (STATUS.VOVCH)

This status indicates whether the battery voltage is higher or lower than the overcharge level threshold. If the battery voltage rises above Vovch then the field set to 1, else it is set to 0.

Bit [1]: Status STOR OVDIS (STATUS.VOVDIS)

This status indicates whether the battery is higher or lower than the overdischarge level threshold. If the battery voltage goes below Vovdis then the field set to 1, else it is set to 0.

8.8.12. Average Power Monitoring Data Registers (APMx)

The APMx (0x0E, 0x0F, 0x10) registers contain the Average Power Monitoring data. Depending on the mode of the APM configured in the APM control register (APM), data is processed differently:

- **Pulse Counter Mode**: the number of pulses is distributed within the registers described in Table 21.

APM0 Register (0x0E)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[7:0]							

APM1 Register (0x0F)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[15:8]							

APM2 Register (0x10)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[23:16]							

Table 21: APMx registers in Pulse Counter Mode

- **Power Meter Mode**: the energy value E_{APM} in nano-Joule is determined by left bit-shifting (SHIFT bits) the value in the DATA field (see Table 23) and applying the following formula:

$$E_{APM} = (DATA \ll SHIFT) \cdot \alpha$$

L_{DCDC}	V_{SRC}	α
3.3 µH	0.25 V to 0.70 V	0.16886
	0.70 V to 1.47 V	0.19774
4.7 µH	0.25 V to 0.70 V	0.13658
	0.70 V to 1.47 V	0.15930
6.8 µH	0.25 V to 0.70 V	0.08817
	0.70 V to 1.47 V	0.10166

Table 22: APM to nano-Joule conversion factor

NOTE: the conversion ratio α is proportional to the inductance of L_{DCDC}. Values from Table 22 are valid for the nominal values stated.

APM0 Register (0x0E)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[7:0]							

APM1 Register (0x0F)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[15:8]							

APM2 Register (0x10)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
SHIFT[3:0]				DATA[19:16]			

Table 23: APMx registers in Power Meter Mode

8.8.13. Temperature Data Register (TEMP)

This field contains the result of the ADC acquisition for the temperature monitoring. The voltage at the terminals of the voltage divider can be derived by applying the following equation, with V_{REF} = 1 V:

$$V_{TH} = \frac{V_{REF} \cdot THRESH}{256}$$

Or, in order to make a comparison with the table in the thermistor data sheet, it is possible to find the impedance of the thermistor:

$$R_{TH} = R_{DIV} \cdot \frac{THRESH}{256 - THRESH}$$

8.8.14. Battery Voltage Register (STO)

The STO (0x12) contains the 8 bits result from the ADC acquisition of the battery voltage. To convert the result to Volts, the following equation is applied.

$$V_{STO} = \frac{4.8V \cdot DATA}{256}$$

8.8.15. Source Voltage Register (SRC)

The SRC (0x13) register contains data reflecting the voltage level at which the input of the AEM10900 is regulated, resulting from the MPPT evaluation. To convert this value in Volts refer to Table 24.

SRC.DATA						
Value						Voltage Level
0	0	0	1	0	1	0.10 V
0	0	0	1	1	0	0.11 V
0	0	0	1	1	1	0.12 V
0	0	1	0	0	0	0.14 V
0	0	1	0	0	1	0.16 V
0	0	1	0	1	0	0.17 V
0	0	1	0	1	1	0.19 V
0	0	1	1	0	0	0.20 V
0	0	1	1	0	1	0.22 V
0	0	1	1	1	0	0.23 V
0	0	1	1	1	1	0.25 V
0	1	0	0	0	0	0.27 V
0	1	0	0	0	1	0.28 V
0	1	0	0	1	0	0.30 V
0	1	0	0	1	1	0.32 V
0	1	0	1	0	0	0.35 V
0	1	0	1	0	1	0.38 V
0	1	0	1	1	0	0.41 V
0	1	0	1	1	1	0.44 V
0	1	1	0	0	0	0.47 V
0	1	1	0	0	1	0.50 V
0	1	1	0	1	0	0.53 V
0	1	1	0	1	1	0.56 V
0	1	1	1	0	0	0.59 V
0	1	1	1	0	1	0.62 V
0	1	1	1	1	0	0.65 V
0	1	1	1	1	1	0.68 V

SRC.DATA						
Value						Voltage Level
1	0	0	0	0	0	0.71 V
1	0	0	0	0	1	0.74 V
1	0	0	0	1	0	0.77 V
1	0	0	0	1	1	0.80 V
1	0	0	1	0	0	0.83 V
1	0	0	1	0	1	0.86 V
1	0	0	1	1	0	0.89 V
1	0	0	1	1	1	0.92 V
1	0	1	0	0	0	0.95 V
1	0	1	0	0	1	0.98 V
1	0	1	0	1	0	1.02 V
1	0	1	0	1	1	1.05 V
1	0	1	1	0	0	1.08 V
1	0	1	1	0	1	1.11 V
1	0	1	1	1	0	1.14 V
1	0	1	1	1	1	1.17 V
1	1	0	0	0	0	1.20 V
1	1	0	0	0	1	1.23 V
1	1	0	0	1	0	1.26 V
1	1	0	0	1	1	1.29 V
1	1	0	1	0	0	1.32 V
1	1	0	1	0	1	1.35 V
1	1	0	1	1	0	1.38 V
1	1	0	1	1	1	1.41 V
1	1	1	0	0	0	1.44 V
1	1	1	0	0	1	1.47 V
1	1	1	0	1	0	1.50 V

Table 24: Source regulation configuration pins

8.9. External Components

8.9.1. Storage element

The storage element of the AEM10900 must be a rechargeable battery, which size should be chosen so that its voltage does not fall below V_{OVDIS} even during occasional current peak from the battery to the load connected on it. To keep the chip functionality, minimum voltage on STO pin shall never fall below 2.8V.

The monitoring of the storage element is done periodically. It is therefore possible that the storage element may be overloaded if it is incorrectly sized.

It is advisable to buffer the battery with a capacitor C_{STO} if the internal resistance of the battery is high, to ensure that the current pulled from the battery by the application circuit does not ever make the battery voltage fall below 2.8 V.

If a disconnection of the battery is expected (e.g. because of a user removable connector), the PCB should include a decoupling capacitor to avoid over-voltage and under-voltage during that battery disconnection. The minimum value of this capacitor depends on various parameters such as the source power, the application current, etc.

A minimal decoupling capacitor of 22 µF is recommended anyway to obtain optimal DCDC converter efficiency when using high ESR battery, or when measuring efficiency using laboratory equipments such as source measurement units (SMU).

8.9.2. External inductor information

L_{DCDC}

The AEM10900 operates with one standard miniature inductor. L_{DCDC} must comply to the following:

- Peak current rating must be at least 1 A for a 3.3 µH inductor in high-power mode and 500 mA if high-power mode is disabled. Current rating decreases linearly when inductor value increases.
- Switching frequency must be at least 10 MHz.
- ESR as low as possible as it has a strong influence on DCDC efficiency.
- The recommended value for optimal efficiency is 6.8 µH.

8.9.3. External capacitors information

C_{SRC}

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage variations when the buck-boost converter is active. The recommended value is 10 µF.

C_{INT}

This capacitor acts as an energy buffer for the internal voltage supply. The recommended value is 3.3 µF.

8.9.4. Optional external components for thermal monitoring

The following components are required for the thermal monitoring:

- One resistor, typ. 22 kΩ ±20% (PNRC0402FR-0722KL)
- One NTC thermistor, typ. R0 = 10 kΩ ±5% and Beta = 3380 K ±3% (NCP15XH103J03RC)

8.9.5. Optional pull-up resistors for the I²C interface

SDA and SCL must be pulled-up by resistors (1 kΩ) if the I²C interface is used. The value must be determined according to the I²C mode used.

9. Typical Application Circuits

9.1. Example Circuit 1

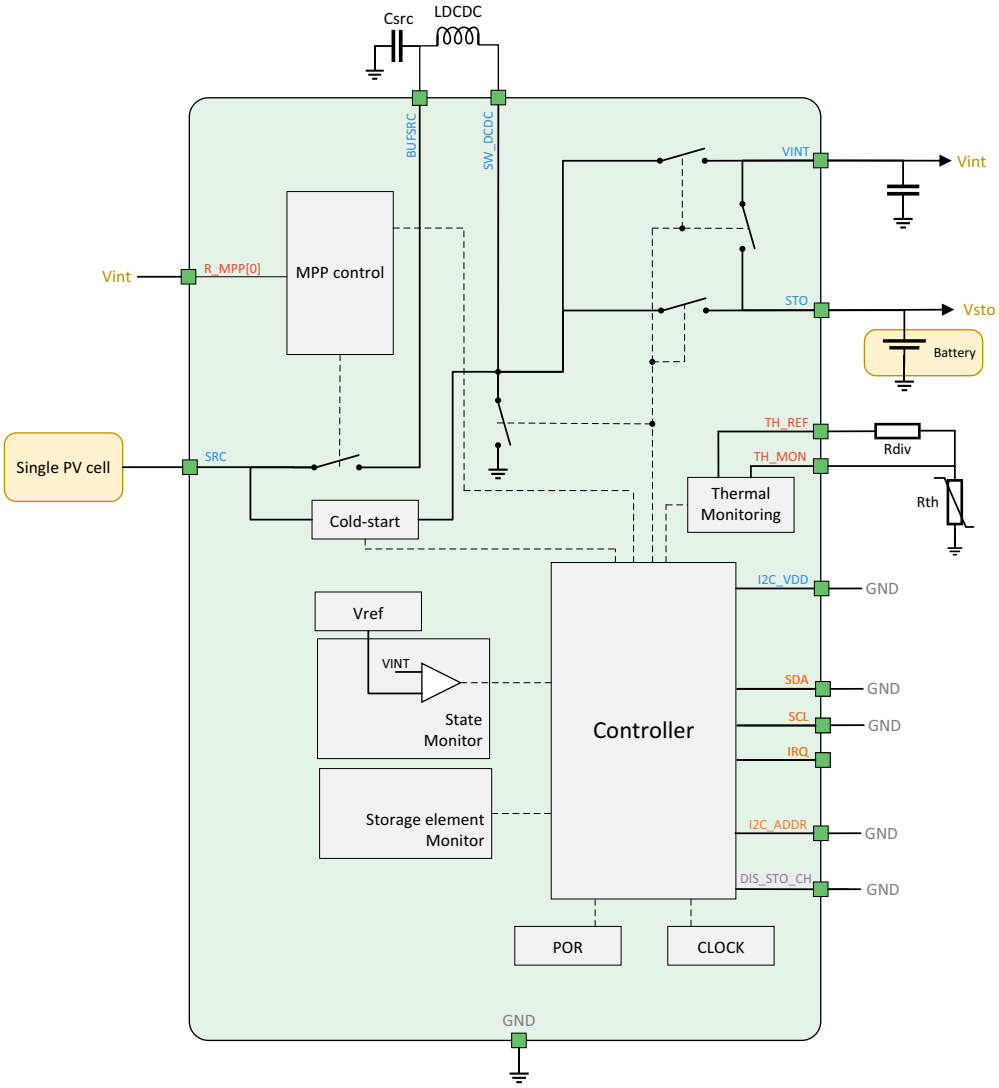


Figure 11: Typical application circuit 1

The circuit is an example of a system with solar energy harvesting with the AEM10900 (Package WLCSP16). It uses a Li-ion rechargeable battery as energy storage.

- Energy source: PV cell
- R_MPP[0] = H: The MPP ratio is set to 80%
- T_MPP[1:0]: VOC timing: 2 ms; MPP evaluation period: 256 ms
- STO_CFG[2:0]: The storage element is a Li-ion battery
- V_{OVCH} = 4.12 V
- V_{OVDIS} = 3.01 V
- The thermal monitoring is used with a default threshold value (TEMPCOLD = 0°C, TEMPHOT = 45°C) with R_{DIV} = 22 kΩ and R_{TH}: NCP15XH103J03RC.
- The I²C communication is not used.
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled

9.2. Example Circuit 2

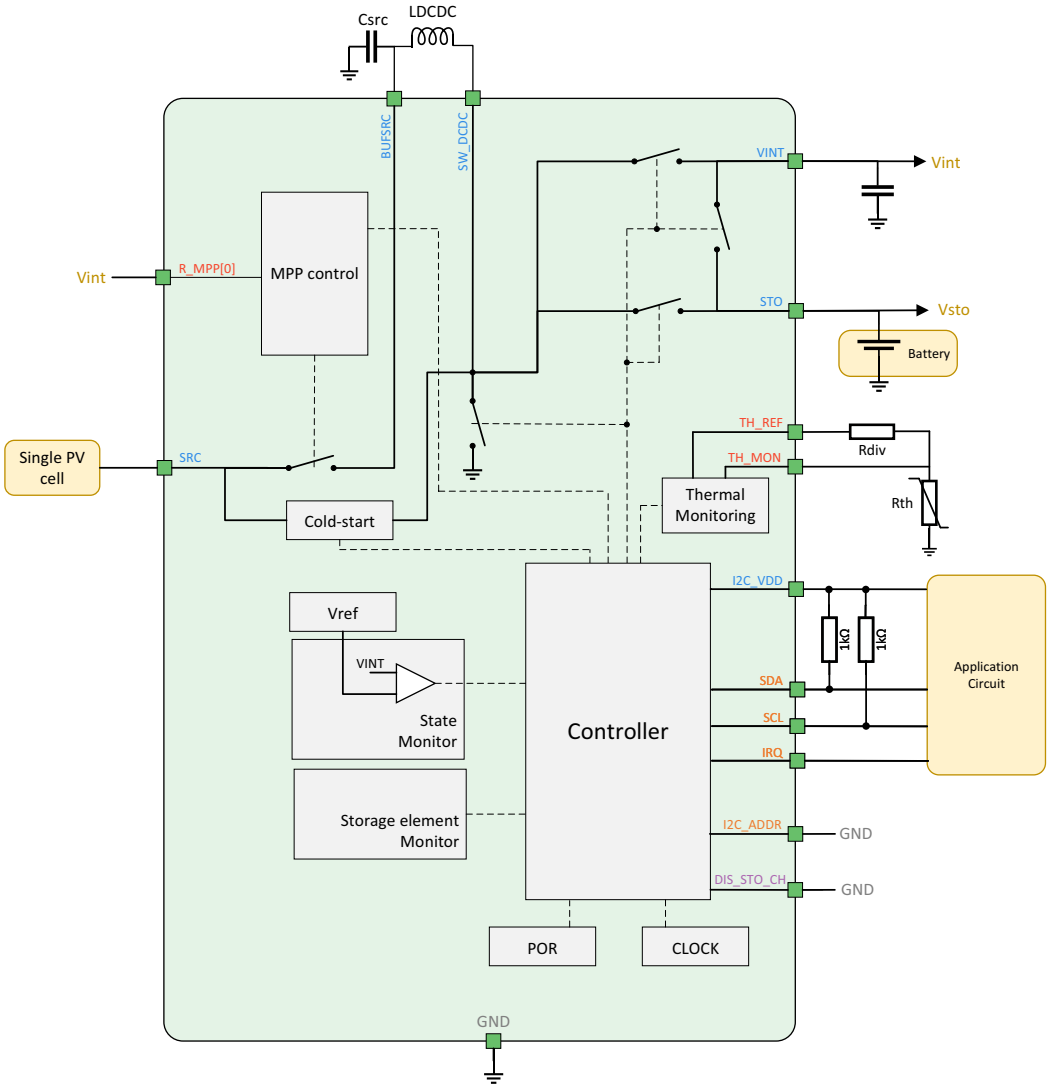


Figure 12: Typical application circuit 2

The circuit is a example of a system with solar energy harvesting with the AEM10900 (Package WLCSP16). It uses a NiCd 3 cells battery as storage element. Before to configure the registers, the AEM have the same configuration as the example circuit 1.

- Energy source: PV cell
- R_MPP[2:0]: Configured through the I²C communication (MPP ratio = 90%)
- T_MPP[1:0]: Configured through the I²C communication (MPP timing = 2ms/128ms)
- STO_CFG[2:0]: Configured through the I²C communication
- V_{OVCH} = 4.12 V
- V_{OVDIS} = 3.30 V
- The thermal monitoring is used and the thresholds are configured through the I²C communication (Cold threshold = 10°C, Hot threshold = 60°C with R_{DIV} = 22 kΩ and R_{TH}: NCP15XH103J03RC.)
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled

Register Address	Register Name	Value
0x01	MPPTCFG	0101 0001
0x02	VOVDIS	0011 0010
0x03	VOVCH	0011 0011
0x04	TEMPCOLD	0111 0100
0x05	TEMPHOT	0001 1111

Table 25: Typical Application Circuit 2 Register Settings

NOTE: a configuration tool is available on the website. It helps the user to read and write on the register.

9.3. Circuit Behavior

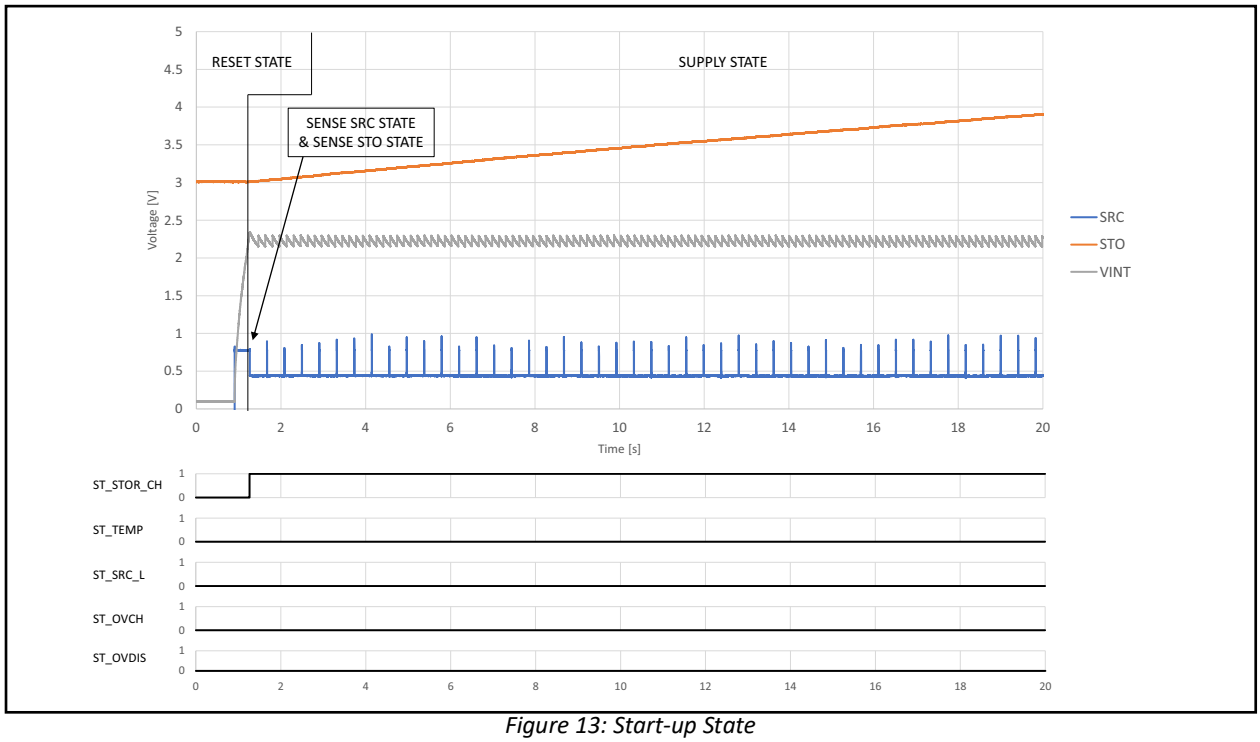


Figure 13: Start-up State

STO_CFG[2:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V), DIS_STO_CH = GND, KEEP_ALIVE = H.

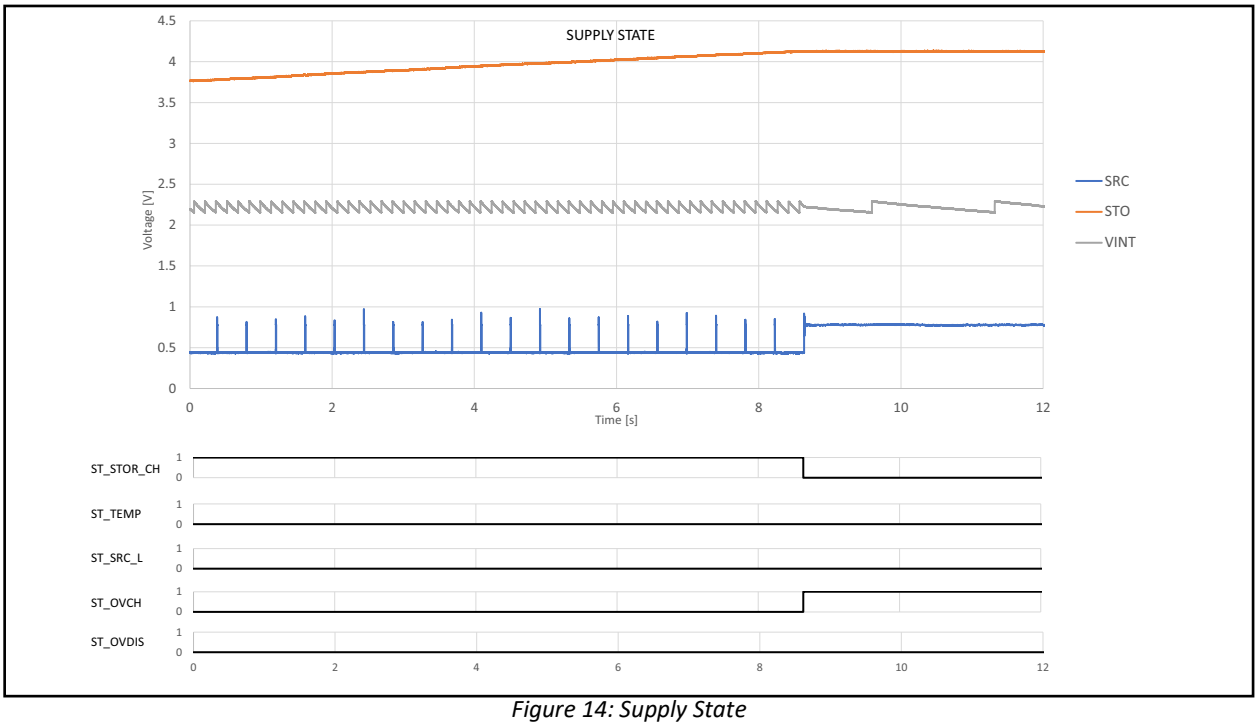


Figure 14: Supply State

STO_CFG[2:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V), DIS_STO_CH = GND, KEEP_ALIVE = H.

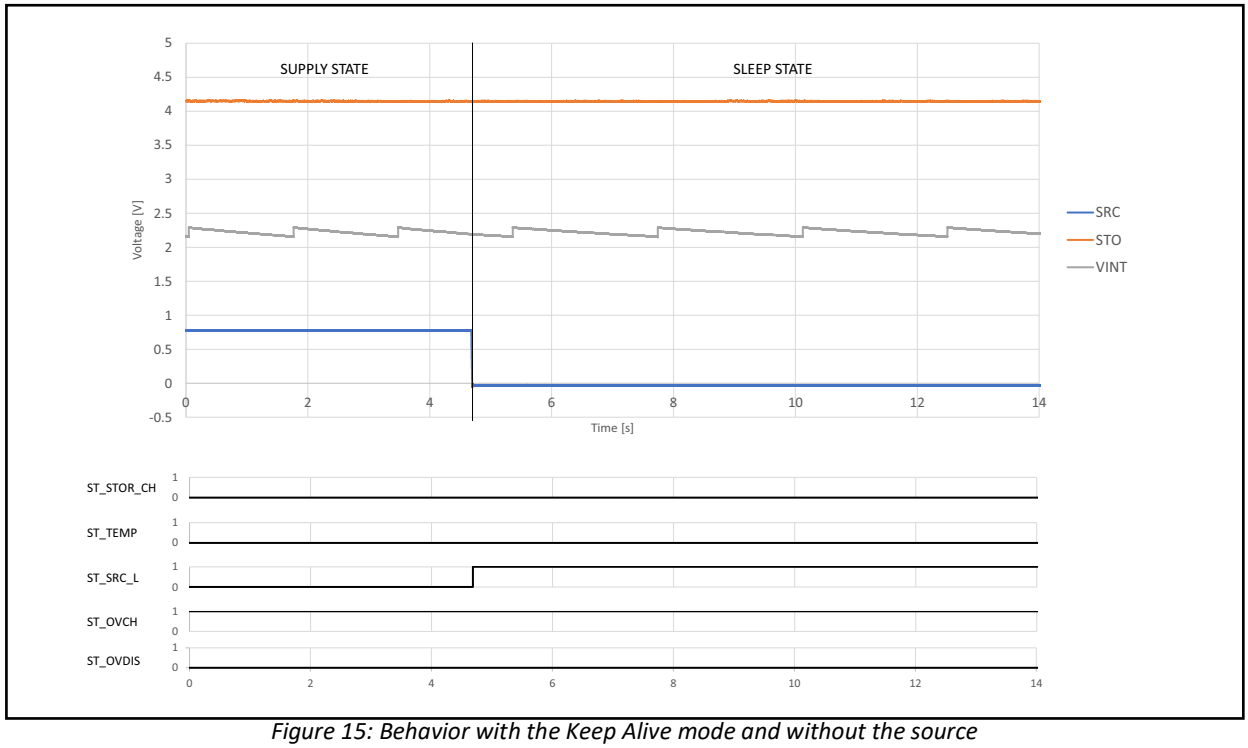


Figure 15: Behavior with the Keep Alive mode and without the source

STO_CFG[2:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V)(stop after ~4.5sec), DIS_STO_CH = GND, KEEP_ALIVE = H.

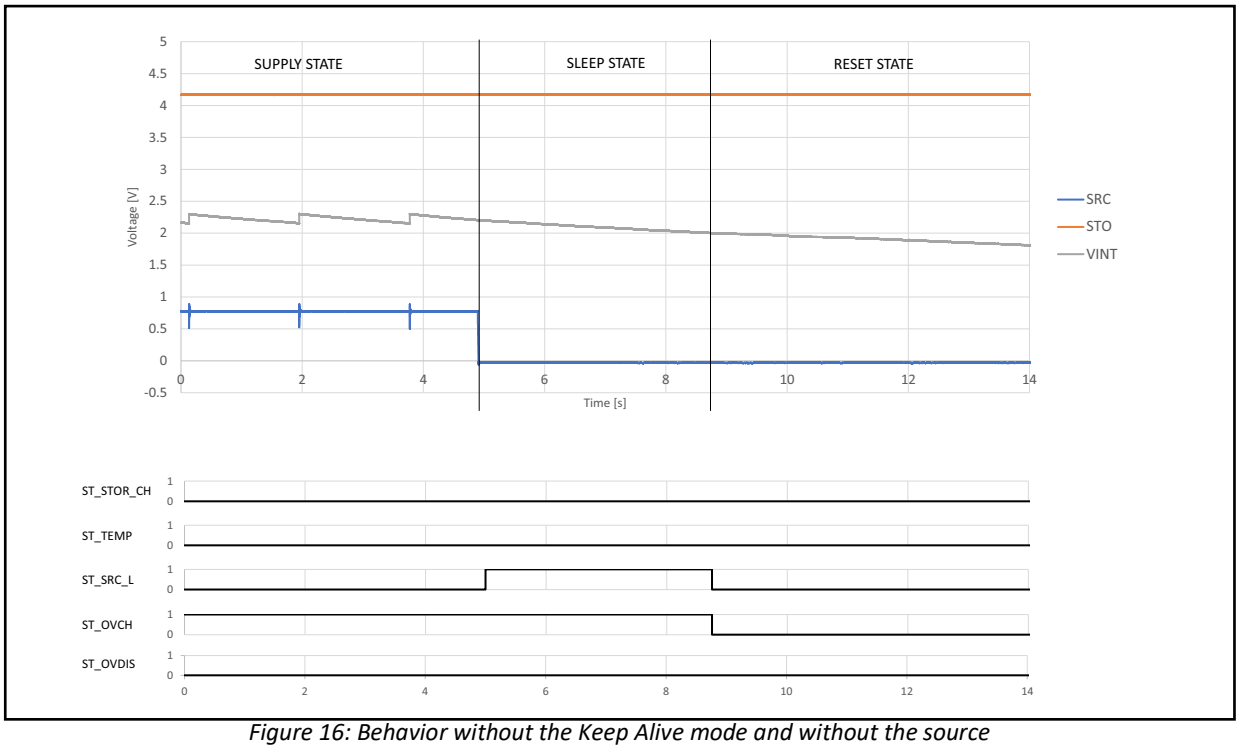


Figure 16: Behavior without the Keep Alive mode and without the source

STO_CFG[2:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V)(stop after ~5sec), DIS_STO_CH = GND, KEEP_ALIVE = H.

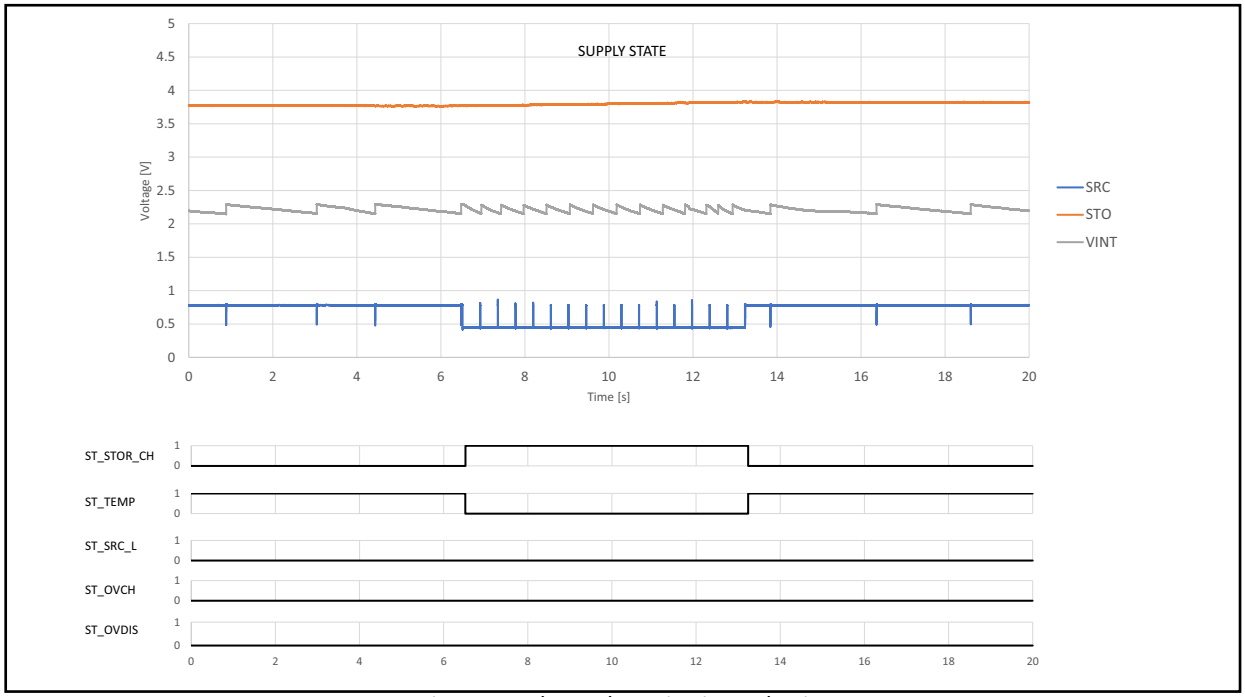


Figure 17: Thermal Monitoring Behavior

STO_CFG[2:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V)(stop after ~5sec), DIS_STO_CH = GND, KEEP_ALIVE = H. The temperature is lower than 0°C before 6.5s and after 13.2s.

10. Performance Data

10.1. DCDC Conversion Efficiency

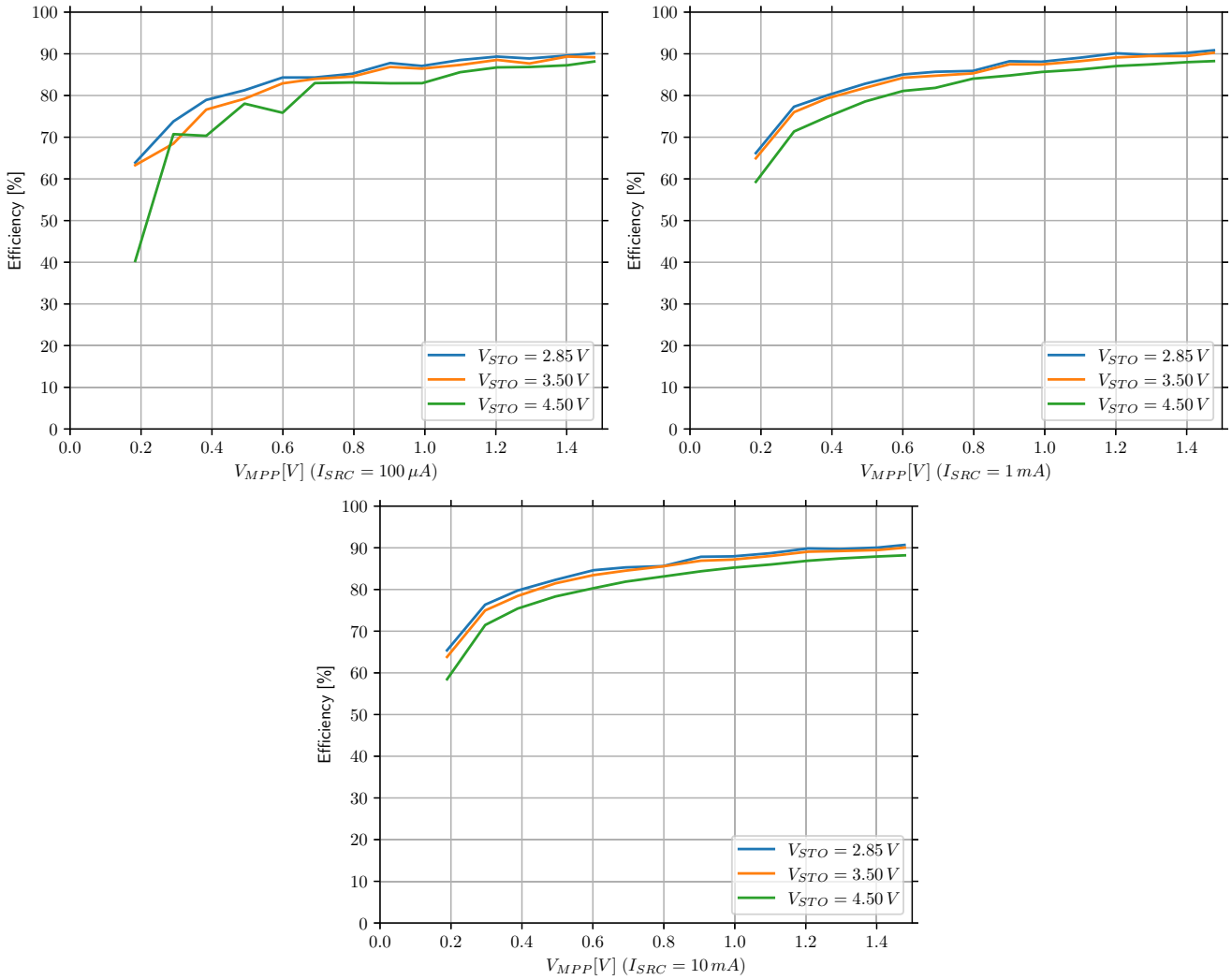


Figure 18: DCDC Conversion Efficiency (LDCDC: TDK VLS252012HBX-6R8M-1)

10.2. Quiescent Current

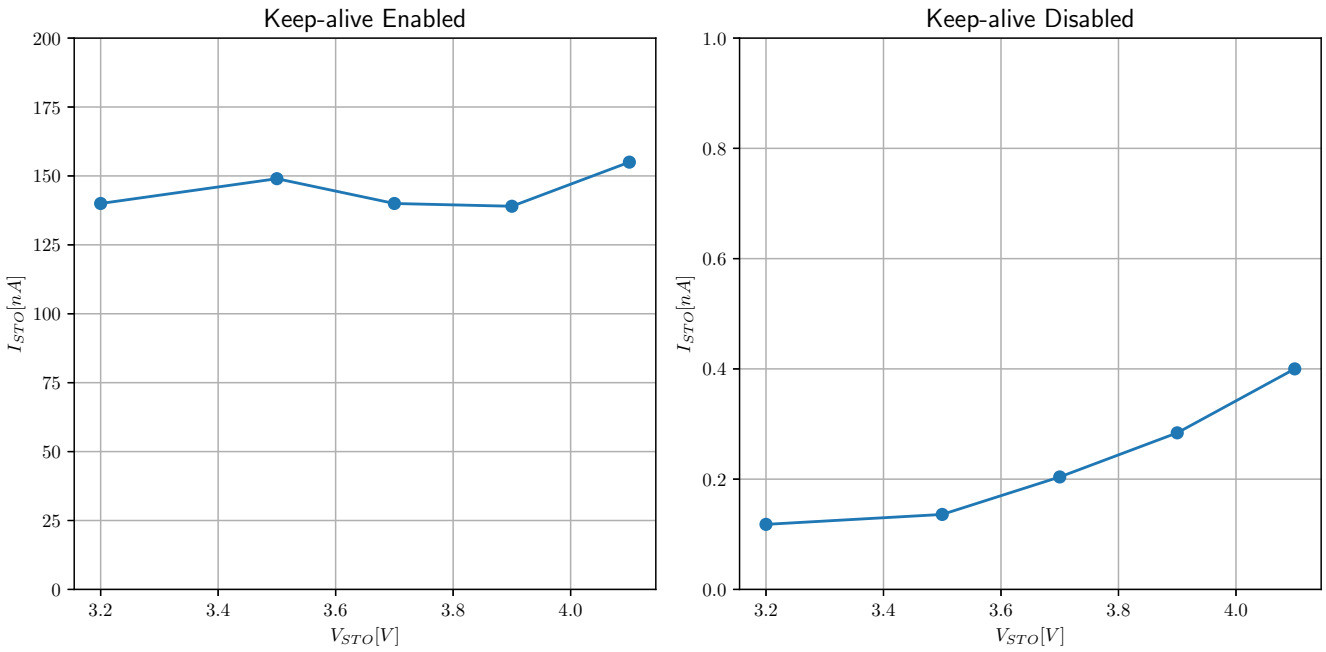


Figure 19: Quiescent Current

11. Package Information

11.1. Wafer Level Chip Scale Package (WLCSP16 2x2mm)

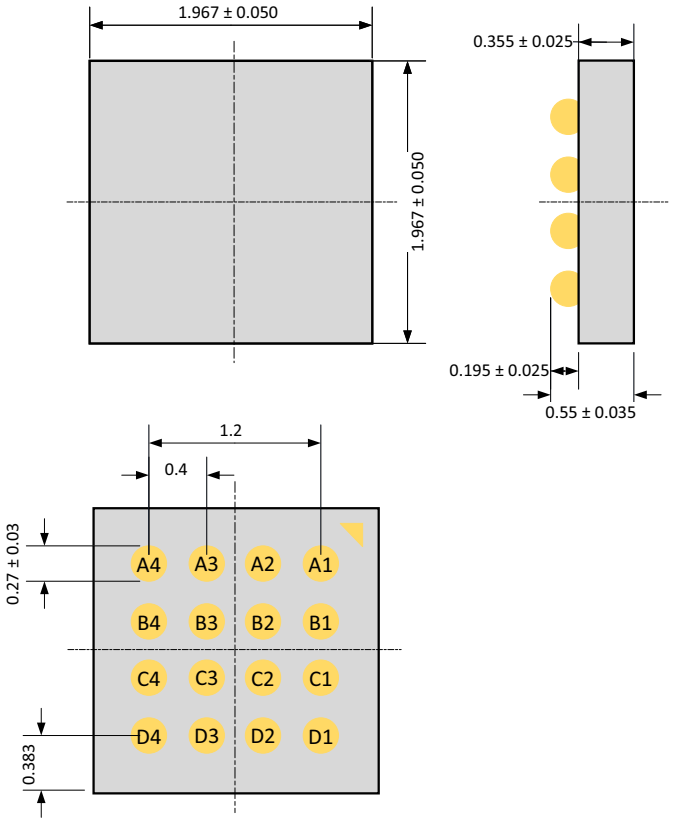


Figure 20: WLCSP16 2x2mm

11.2. WLCSP16 Board Layout

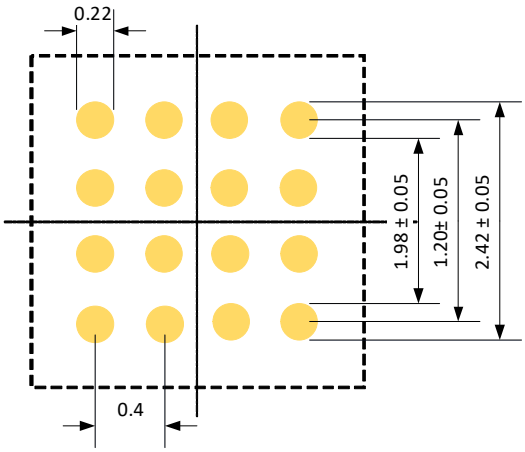


Figure 21: WLCSP16 board layer

11.3. Plastic quad flatpack no-lead (QFN28 4x4mm)

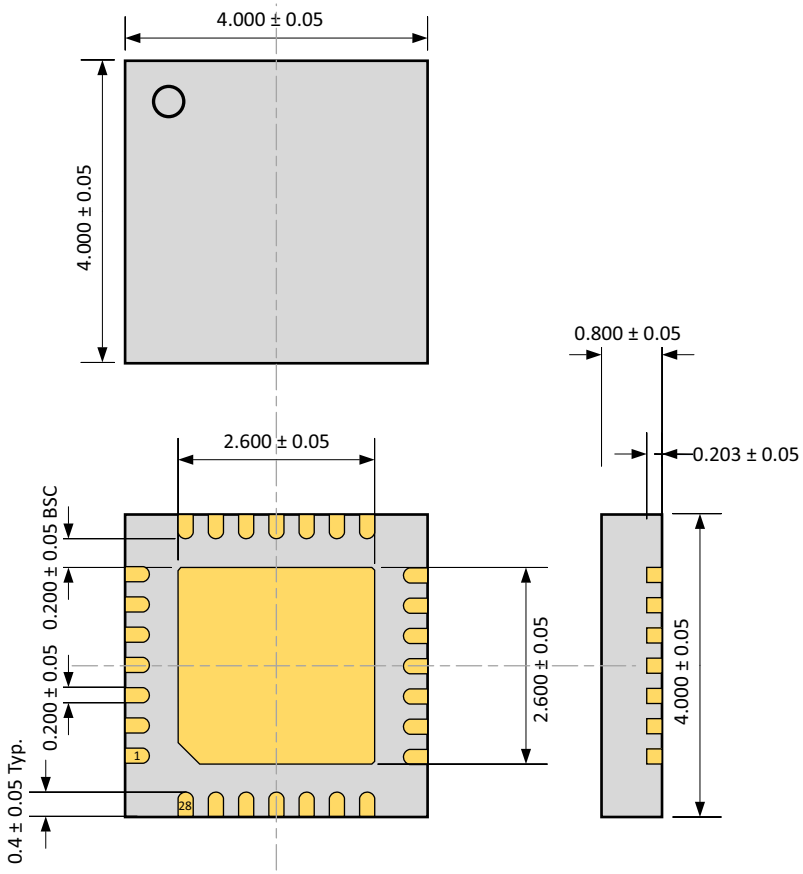


Figure 22: QFN28 4x4 mm

11.4. QFN28 Board Layout

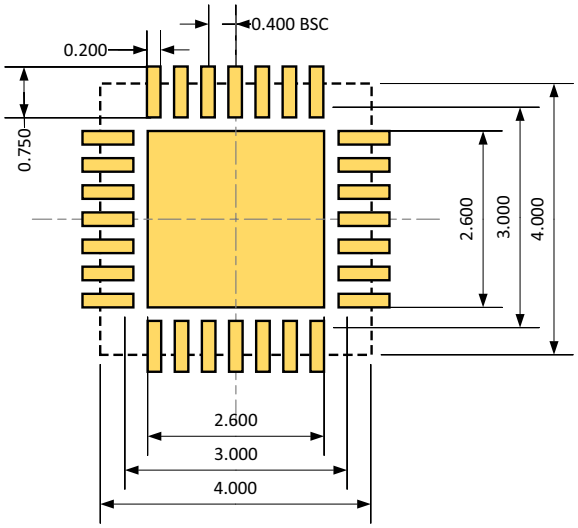


Figure 23: QFN28 4x4 mm board layout

12. Minimum BOM

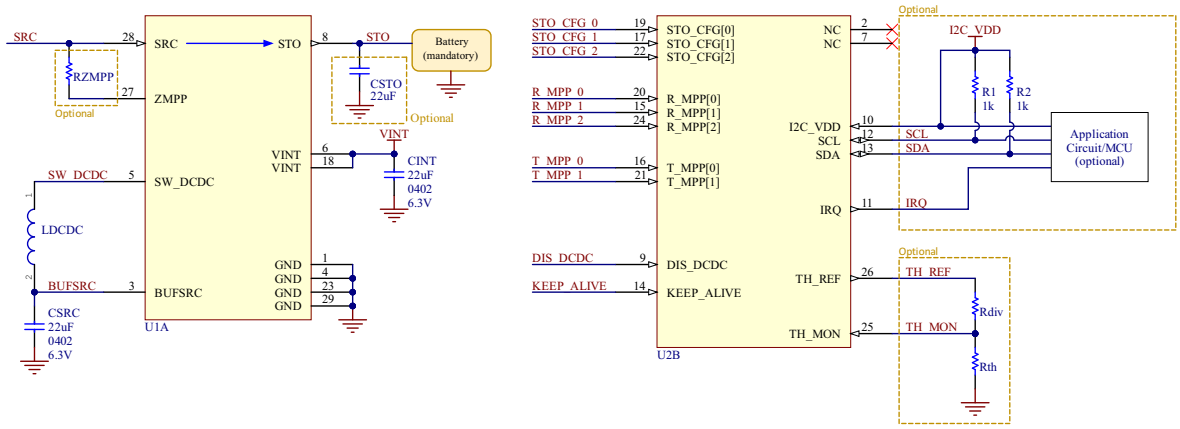


Figure 24: AEM10900 schematic

	Designator	Description	Quantity	Manufacturer	Part Number
Mandatory	U1	AEM10900	1	e-peas	order at sales@e-peas.com
	Battery	Battery with 2.8 V min. voltage	1	To be defined by user	
	LDCDC	Power inductor 6.8 µH 1.15A 1008	1	TDK	VLS252012HBX-6R8M-1
	CSRC	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
	CINT	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
Optional	CSTO	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
	RZMPP	Resistor for ZMPP functionality	1	To be defined by user	
	R1, R2	Pull-up 1kΩ Resistors for I²C interface	2	Yageo	AC0603FR-071KL
	Rth	10kΩ NTC thermistor for temperature monitoring	1	Murata	NCP15XH103J03RC
	Rdiv	Resistor 22kΩ 1%	1	Yageo	PNRC0402FR-0722KL

Table 26: AEM10900 bill of material

13. Glossary

V_{STO}

Voltage at the STO pin.

$V_{SRC,REG}$

Target regulation voltage at the SRC pin.

$V_{SRC,CS}$

Minimum source voltage required for cold start.

V_{SRC}

Voltage at the SRC pin.

V_{OVDIS}

Over-discharge voltage at the STO pin.

V_{OVCH}

Over-charge voltage at the STO pin.

V_{OC}

Open-circuit voltage of the harvester connected to the SRC pin.

V_{MPP}

Target regulation voltage on SRC when extracting power.

V_{INT}

AEM10900 internal circuit voltage supply.

$T_{RESET,SUPPLY}$

From SUPPLY STATE: delay before reset when no energy on SRC and Keep-alive functionality disabled, or if Keep-alive is enabled but the battery voltage dropped below V_{OVDIS}.

$T_{RESET,SLEEP}$

Same as $T_{RESET,SUPPLY}$ from SLEEP STATE.

$P_{SRC,CS}$

Minimum power available on SRC for the AEM10900 to coldstart.

$I_{QSUPPLY}$

Quiescent current on VINT when the AEM10900 is in SUPPLY STATE.

I_{QSLEEP}

Quiescent current on VINT when the AEM10900 is in SLEEP STATE.

I_{QSTO}

Quiescent current on STO when Keep-alive functionality is disabled.

R_{TH}

Thermistor used for the AEM10900 thermal monitoring feature.

R_{DIV}

Resistor that creates a resistive voltage divider with R_{TH}.

C_{INT}

VINT pin decoupling capacitor.

C_{SRC}

BUFSRC pin decoupling capacitor.

L_{DCDC}

DCDC converter inductor.

R_{SCL} / R_{SDA}

Respectively, I²C SCL and SDA pin pull-up resistors.

R_{ZMPP}

Resistor that defines the AEM10900 DCDC converter input resistance when used in ZMPP mode.

T_{MPPT}

Maximum power point tracking sampling period.

T_{VOC}

Duration of the SRC open circuit voltage evaluation.

14. Revision History

Revision	Date	Description
1.0	April, 2021	Creation of the document.
1.1	April, 2021	- Modification of SRC_DATA register value table - Added performance and typical applications
1.2	August, 2022	- Change name of the register and field for the I²C Communication - Change the Package and the pinout for the WLCSP package

1.3	January, 2023	- Global layout update.
		- First page full rework.
		- Introduction: added details on cold start power and SRC extracting range.
		- Typical electrical characteristics:
		  - Cold start voltage vs. MPP voltage.
		  - Cold start power depending on keep-alive enabling.
		- Recommended operating conditions: refined LDCDC value range.
		- MPPT description rework.
		- APM description completed.
		- Keep-alive description improved.
		- IRQ pin: added dedicated section.
		- States description improved.
		- Configuration by pin/registers: clarified.
		- DIS_STO_CH: added dedicated section.
		- Register descriptions: added register names in section titles and improved tables layout.
		- Keep-alive register: added note.
		- Improved register descriptions:
		  - APM related registers.
		  - IRQEN.I2CRDY.
		  - IRQFLG.I2CRDY.
		- External inductor informations: improved.
		- Typical application circuits: improved schematics aesthetics.
		- Improved performance graphs aesthetics.
		- Quiescent current graph: improved aesthetics.
		- Moved “Minimum BOM” section outside “Package” section.
		- Added glossary.
		- Explanations about CSTO influence on efficiency.

1.4	February, 2023	- APM register conversion to energy: replaced formula by Table 22. - I2C_VDD: max. voltage to 2.2 V. - I2C_VDD: more explanation about pin use when using I²C and not using I²C. - Added component part number. - LDCDC from 4.7 µH to 6.8 µH in typical application circuits and in efficiency graphs. - Explanations about CSTO influence on efficiency.

Table 27: Revision History