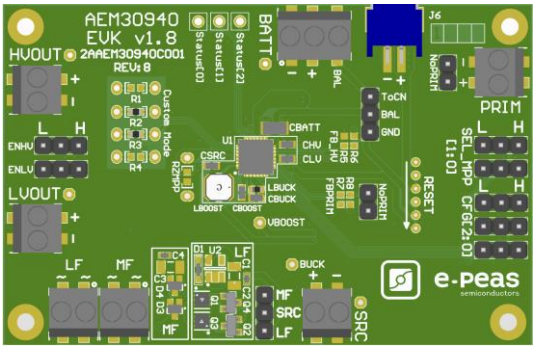
AEM30940
Quick Start Guide EVK



FEATURES

Connectors

- 1 screw connector for the DC source
- 2 screw connectors for AC sources
- 1 screw connector + 1 JST connector for the storage element
- 1 screw connector for primary battery
- 1 screw connector for HVOUT LDO output (80mA @ 1.8 – 4.1 V)
- 1 screw connector for LVOUT LDO output (20mA @ 1.2 or 1.8 V)

Configuration

- 2 headers SELMPP[1:0] to define the MPPT ratio linked to the harvester technology
- 3 headers CFG[2:0] to define the storage element protection levels
- 6 resistor footprints to configure the custom mode (CFG[2:0] = LLL)
- 2 headers to enable/disable the internal LDOs
- 2 headers to disable the primary battery feature
- 1 header to set the dual cell supercapacitor BAL feature
- 1 resistors footprint to use the ZMPP feature (constant impedance)

Size

- 76mm x 49mm
- 4 x M2.5 mounting holes

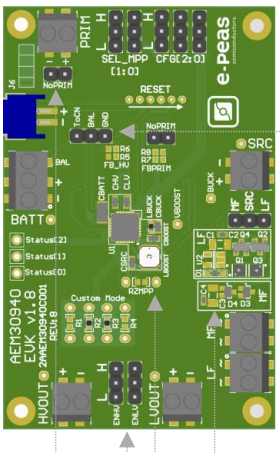
SUPPORT PCB

BOM around the AEM30940

Designator	Description	Quantity	Manufacturer	Part Number
U1	AEM30940	1	e-peas	order at sales@e-peas.com
L_{BOOST}	Power Inductor 22 µH - 0,65 A - LPS4018	1	Coilcraft	LPS4018-223MR
L_{BOOST} (alt.)	Power Inductor 10 µH - 0,90 A - LPS4018	1	Coilcraft	LPS4018-103MR
L_{BOOST} (alt.)	Power Inductor 10 µH - 0,84 A - 3015	1	Würth	744 040 321 00
C_{BOOST}	Ceramic Cap 22 µF, 10 V, 20%, X5R, 0603	1	Murata	GRM188R61A226ME15D
L_{BUCK}	Power Inductor 10 µH - 0,25 A - 0603	1	TDK	MLZ1608M100WT
C_{BUCK}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{SRC}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{HV}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{LV}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{BATT}	Ceramic Cap 150 µF, 6.3 V, 20%, X5R, 1206	1	Murata	GRM31CR60J157ME11L

Footprint & Symbol: Available in the datasheet

STEP 1: Configure the AEM30940



- **MPPT ratio:** SELMPP[1:0]

SELMPP[1]	SELMPP[0]	Vmpp/Voc
L	L	50%
L	H	65%
H	L	80%
H	H	ZMPP

- **Storage element voltages protection:** CFG[2:0]

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode				1.8 V	

- **BAL option:** Select “ToCn” to use the balancing or “GND” to disable it

- **PRIM option:** Connect both headers “NoPRIM” to disable the primary feature or remove them if a primary battery is connected. Define the lower limit voltage on the primary battery using R7 and R8:

  - RP = R7 + R8
  - 100 kΩ ≤ RP ≤ 500 kΩ
  - R7 = ($\frac{Vprim\_min}{4}$ * RP) / 2.2 V
  - R8 = RP – R7

- **ZMPP resistors footprint**

- **LDOs Outputs Voltages:** ENHV (HVOUT) – ENLV (LVOUT)

ENLV	LVOUT
L	Disabled
H	Enabled

ENHV	HVOUT
L	Disabled
H	Enabled

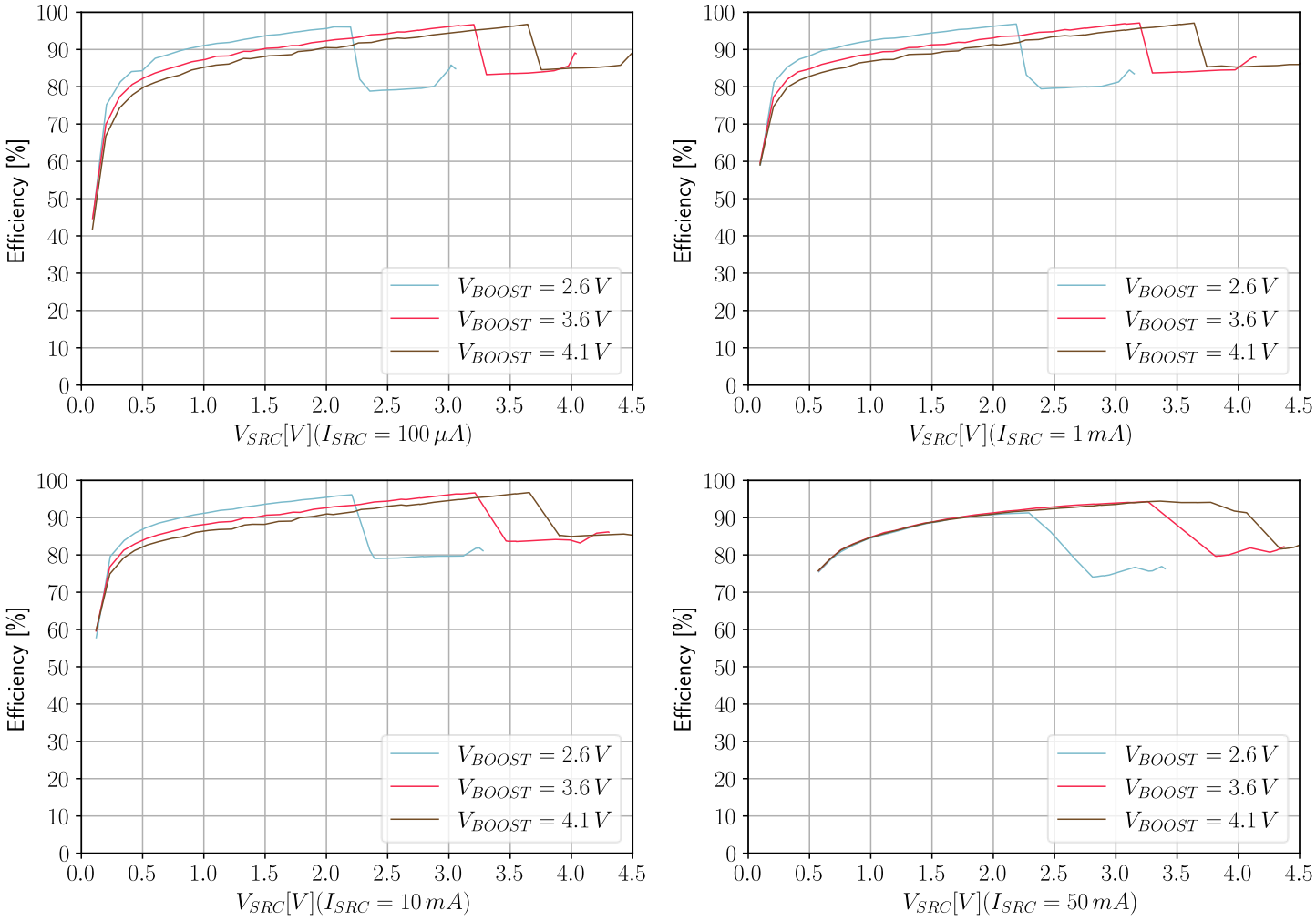
- **DIODE BRIDGE RECTIFIER (BAT54)** with zener diode footprint at the output :
  R13 & R19 resistors are mandatory

STEP 2: Connect the storage element (and the primary battery)

STEP 3: Connect the load(s) to HVOUT / LVOUT

STEP 4: Connect the harvester

Internal boost efficiency Vs. input voltage (LBOOST = 22 µH):



STEP 5: Check the status

Status pins		
STATUS[2]	19	Logic output. Asserted when the AEM performs a MPP evaluation.
STATUS[1]	20	Logic output. - HIGH: - during T_{CRIT} when in SHUTDOWN MODE. - as long as in PRIMARY BATTERY MODE. - LOW otherwise.
STATUS[0]	21	Logic output. Asserted when the LDOs can be enabled.