



Ultra Efficient Dual Sources Energy Manager with Ratio/Constant Voltage Regulation, Regulated Buck Output and 5 V CC/CV Charger

Features and Benefits

Dual sources inputs

- Optimized boost operation for each source.
- Efficiency above 90 % on each source.
- Harvests from 120 mV after cold start.
- Simultaneous harvesting from both sources.
- Up to 135 mA current extracted from the harvester.

Maximum Power Point Tracking

- Both sources are configurable to constant voltage mode or to open circuit voltage ratio mode.
- Optimal harvesting from a multiple combinations of harvesters (PV cells, RF, vibration, pulsed sources...).

Cold start from 275 mV / 1.5 μ W input

- Startup at ultra-low power from each harvesting source input.

Selectable overdischarge and overcharge protection

- Supports various types of rechargeable batteries (LiC, Li-ion, LiPo, Li-ceramic pouch...).

Regulated output for application circuit

- Buck regulator with efficiency above 90 %.
- Selectable output voltage between 0.6 V and 2.5 V.
- Output current up to 100 mA.

Thermal monitoring

- Battery protection against over-temperature and under-temperature during charging and discharging, independently.

Average Power Monitoring

- Measures how much energy has been transferred to the battery by each source and the energy drained from the battery to supply the application circuit.

System configuration by GPIO or I²C communication

- All settings are dynamically configurable through GPIO or I²C (Fast Mode Plus).
- System data is available through I²C.

Shipping mode

- Disables charging and discharging battery during shipment.

External 5 V charging capability

- Extra charging input for 5 V power supplies.
- CC/CV charging with configurable current limit in CC mode (max. 135 mA).
- Provides a fast charging alternative when no source is available for a long time.

Applications

Smart home	Industrial sensor
Smart building	Retail
Edge IoT	PC accessories

Description

The AEM13920 is a fully integrated and compact power management circuit that extracts DC power from two harvesting sources to store energy in a rechargeable battery and supply an application circuit. A 5 V input can also be used to charge the battery (e.g. if the battery gets depleted). This compact and ultra-efficient battery charger allows for extending battery lifetime and eliminating the primary energy storage in a large range of applications.

Both sources implement Maximum Power Point Tracking (MPPT) based on open circuit voltage ratio as well as constant source voltage regulation features, allowing for harvesting the maximum power available from each source to charge the storage element.

With its unique cold-start circuit, it can start operating with an input voltage as low as 275 mV (min. 1.5 μ W power).

The configurable protection levels determine the storage element voltage protection thresholds to avoid overcharging and overdischarging the storage element and thus damaging it. No external components are required to set those levels.

Thermal monitoring protects the storage element. Average Power Monitoring system (APM) allows the application circuit to get an estimate of the energy harvested from each source to the battery and from the battery to the application circuit. A shipping mode is available to avoid charging and discharging of the storage element during shipping or storage.

A buck regulator with selectable output voltage allows an application circuit to be supplied with high efficiency.

I²C communication allows users to control every setting of the AEM13920 from the application circuit MCU.

Device Information

Part Number	Package	Body size
10AEM13920J0000	QFN 40-pin	5x5mm

Evaluation Board

Part number
2AAEM13920J051

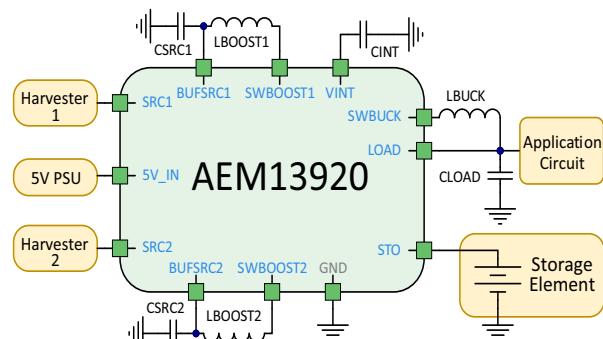




Table of Contents

1. Introduction	9
2. Pin Configuration and Functions	10
3. Specifications	13
3.1. Absolute Maximum Ratings	13
3.2. ESD Ratings	13
3.3. Thermal Resistance	13
3.4. Electrical Characteristics at 25 °C	14
3.5. Recommended Operation Conditions	16
3.6. Typical Characteristics	18
3.6.1. Boost Converter Conversion Efficiency	18
3.6.2. Buck Converter Conversion Efficiency	19
4. Functional Block Diagram	20
5. Theory of Operation	21
5.1. Cold-Start Circuits	21
5.2. Boost Converters	21
5.2.1. Operation Principle	21
5.2.2. Maximum Power Point Tracking	22
5.2.2.1. Open-Circuit Voltage Ratio	22
5.2.2.2. ZMPP	22
5.2.3. Source Constant Voltage Regulation	22
5.2.4. Automatic High-Power Mode	23
5.2.5. Using Both Boost Converters in Parallel	23
5.3. Buck Converter	24
5.4. Thermal Monitoring	25
5.5. Average Power Monitoring	25
5.6. IRQ Pin	25
5.7. 5 V Charger	25
5.8. Shipping Mode	25
5.9. State Machine Description	26
5.9.1. Reset State	26
5.9.2. Sense STO State	26
5.9.3. Start State	27
5.9.4. Supply State	27
5.9.5. OVDIS State	27
5.9.6. Sleep State	27
6. System Configuration	28
6.1. Configuration Pins and I ² C	28
6.1.1. Configuration Pins	28
6.1.2. Configuration by I ² C	28
6.2. Maximum Power Point Tracking	28
6.3. Source Constant Voltage Regulation	29
6.4. Storage Element Thresholds	30
6.5. Boost Converter Timings	31
6.6. Buck Converter	31



6.6.1. Load Voltage	31
6.6.2. Buck Converter Timings	31
6.7. Thermal Monitoring	31
6.8. 5 V Charger	32
6.9. Shipping Mode	32
7. I²C Serial Interface Protocol	33
8. Register Map	35
9. Registers Configuration	38
9.1. I ² C Control (CTRL)	38
9.2. Version Register (VERSION)	38
9.3. Source Regulation Configuration Registers (SRCxREGUx)	39
9.3.1. SRCxREGU0	39
9.3.2. SRCxREGU1	40
9.3.3. Constant Voltage Configuration	41
9.3.4. MPPT Configuration	42
9.4. Storage Element Threshold Voltages (VOVDIS / VCHRDY / VOVCH)	43
9.4.1. Overdischarge Voltage (VOVDIS)	43
9.4.2. Charge Ready Voltage (VCHRDY)	44
9.4.3. Overcharge Voltage (VOVCH)	45
9.5. Boost Converters (BSTxCFG)	46
9.6. Buck Converter (BUCKCFG)	47
9.7. Temperature Monitoring Enable (TMON)	48
9.8. STO Charge Temperature Monitoring (TEMPCOLDCH and TEMPHOTCH)	48
9.8.1. TEMPCCOLDCH	48
9.8.2. TEMPHOTCH	48
9.9. STO Discharge Temperature Monitoring (TEMPCOLDDIS and TEMPHTDIS)	49
9.9.1. TEMPCCOLDDIS	49
9.9.2. TEMPHTDIS	49
9.10. Source Low Threshold (SRCLOW)	50
9.11. IRQ Enable (IRQENx)	51
9.11.1. IRQENO	51
9.11.2. IRQEN1	52
9.12. IRQ Flags (IRQFLGx)	53
9.12.1. IRQFLG0	53
9.12.2. IRQFLG1	54
9.13. Status (STATUSx)	55
9.13.1. STATUS0	55
9.13.2. STATUS1	55
9.14. Average Power Monitoring Configuration (APM)	56
9.15. SRCx APM Data (APMxSRCx)	57
9.15.1. APM0SRCx	57
9.15.2. APM1SRCx	57
9.15.3. APM2SRCx	57
9.16. BUCK APM Data (APMxBUCK)	58
9.16.1. APM0BUCK	58
9.16.2. APM1BUCK	58
9.16.3. APM2BUCK	58



9.17. APM Error (APMERR)	59
9.18. Temperature Monitoring Data (TEMP)	60
9.19. Storage Element Voltage Data (STO)	60
9.20. Sources Voltage Data (SRCx)	61
10. Typical Application Circuits	62
10.1. Example Circuit 1	62
10.2. Example Circuit 2	64
10.3. Example Circuit 3	66
11. Circuit Behavior	69
11.1. Start Up from SRCx	69
11.1.1. Configuration	69
11.1.2. Observations	70
11.2. Shutdown	71
11.2.1. Configuration	71
11.2.2. Observations	72
11.3. Start Up from 5V_IN	73
11.3.1. Configuration	73
11.3.2. Observations	73
12. Minimum BOM	74
13. Layout	75
13.1. Guidelines	75
13.2. Example	76
14. Package Information	77
14.1. Moisture Sensitivity Level	77
14.2. RoHS Compliance	77
14.3. REACH Compliance	77
14.4. Package Dimensions	78
14.5. Board Layout	79
15. Glossary	80
15.1. SRCx Acronyms	80
15.2. STO Acronyms	80
15.3. VINT Acronyms	80
15.4. I ² C Acronyms	81
15.5. LOAD Acronyms	81
15.6. 5V_IN Acronyms	81
15.7. Various Acronyms	81
16. Revision History	82



List of Figures

Figure 1: Simplified schematic view	9
Figure 2: Pinout diagram	10
Figure 3: Boost converter efficiency with $L_{BOOSTx} = 33 \mu\text{H}$ (Coilcraft LPS4018-333MRB), BSTxCFG.TMULT = 0x02 (x3)	18
Figure 4: Buck (LOAD) converter efficiency with $L_{BUCK} = 10 \mu\text{H}$ (Coilcraft LPS4018-103MRB), BUCKCFG.TMULT = 0x01 (x2)	19
Figure 5: Functional block diagram	20
Figure 6: Simplified schematic view of the boost converters	21
Figure 7: ZMPP connection with both boost converters used in parallel	23
Figure 8: Simplified schematic view of the buck converter	24
Figure 9: AEM13920 state machine	26
Figure 10: TH_REF and TH_MON connections	31
Figure 11: I ² C transmission frame	33
Figure 12: Read and write transmission	34
Figure 13: Typical application circuit 1	62
Figure 14: Typical application circuit 2	64
Figure 15: Typical application circuit 3	66
Figure 16: AEM13920 behavior at start up	70
Figure 17: AEM13920 behavior at shutdown	72
Figure 18: AEM13920 behavior at start up from 5V_IN	73
Figure 19: AEM13920 schematic	74
Figure 20: AEM13920 layout example	76
Figure 21: QFN 40-pin 5x5mm drawing (all dimensions in mm)	78
Figure 22: Recommended board layout for QFN40 package (all dimensions in mm)	79



List of Tables

Table 1: Pins description (part 1)	10
Table 2: Pins description (part 2)	11
Table 3: Pins description (part 3)	12
Table 4: Absolute maximum ratings	13
Table 5: ESD ratings	13
Table 6: Thermal data	13
Table 7: Electrical characteristics (part 1)	14
Table 8: Electrical characteristics (part 2)	15
Table 9: Recommended external components	16
Table 10: Logic input pins and I ² C interface pins connections	17
Table 11: MPPT ratio configuration with SRCx_CFG[2:0] pins	28
Table 12: MPPT timing configuration with SRCx_CFG[4:3] pins	28
Table 13: Configuration of the source constant voltage regulation with SRCx_CFG[4:0] pins	29
Table 14: Storage element configuration with STO_CFG[2:0] pins	30
Table 15: Configuration of LOAD voltage with LOAD_CFG[2:0] pins	31
Table 16: Typical resistor values for setting 5 V charger max. current	32
Table 17: Register map	35
Table 18: CTRL register	38
Table 19: VERSION register	38
Table 20: Summary of SRCxREGUx register fields	39
Table 21: SRCxREGU0 register	39
Table 22: SRCxREGU1 register	40
Table 23: SRCx constant voltage values configured by SRCxREGUx (SRCxREGU0.MODE = 0)	41
Table 24: SRCx MPPT ratio/ZMPP configured by SRCxREGUx (SRCxREGU0.MODE = 1)	42
Table 25: SRCx MPPT sampling duration configured by SRCxREGUx (SRCxREGU0.MODE = 1)	42
Table 26: SRCx MPPT period configured by SRCxREGUx (SRCxREGU0.MODE = 1)	42
Table 27: VOVDIS register	43
Table 28: Storage element V _{OVDIS} configuration by VOVDIS register	43
Table 29: VCHRDY register	44
Table 30: Storage element V _{CHRDY} configuration by VCHRDY register	44
Table 31: VOVCH register	45
Table 32: Storage element V _{OVCH} configuration by VOVCH register	45



Table 33: BSTxCFG registers	46
Table 34: Boost inductor values according to boost timing	46
Table 35: BUCKCFG register	47
Table 36: Buck inductor values according to buck timing	47
Table 37: V_{LOAD} settings by BUCK.VOUT register	47
Table 38: TMON register	48
Table 39: TEMPcoldch register	48
Table 40: TEMPphotch register	48
Table 41: Tempcolddis register	49
Table 42: Tempphotdis register	49
Table 43: SRCLOW register	50
Table 44: V_{SRCLOW} thresholds as configured by the SRCLOW register	50
Table 45: IRQENO register	51
Table 46: IRQEN1 register	52
Table 47: IRQFLG0 register	53
Table 48: IRQFLG1 register	54
Table 49: STATUS0 register	55
Table 50: STATUS1 register	55
Table 51: APM register	56
Table 52: APM0SRCx register	57
Table 53: APM1SRCx register	57
Table 54: APM2SRCx register	57
Table 55: APM0BUCK register	58
Table 56: APM1BUCK register	58
Table 57: APM2BUCK register	58
Table 58: APMERR register	59
Table 59: TEMP register	60
Table 60: STO register	60
Table 61: SRCx register	61
Table 62: Source voltage V_{SRCx} from SRCx.DATA register value (formula)	61
Table 63: Source voltage V_{SRCx} from SRCx.DATA register value (lookup table)	61
Table 64: Summary of I ² C register configuration for typical application circuit 3	68
Table 65: Minimum BOM	74



Table 66: Moisture sensitivity level	77
Table 67: Revision history	82

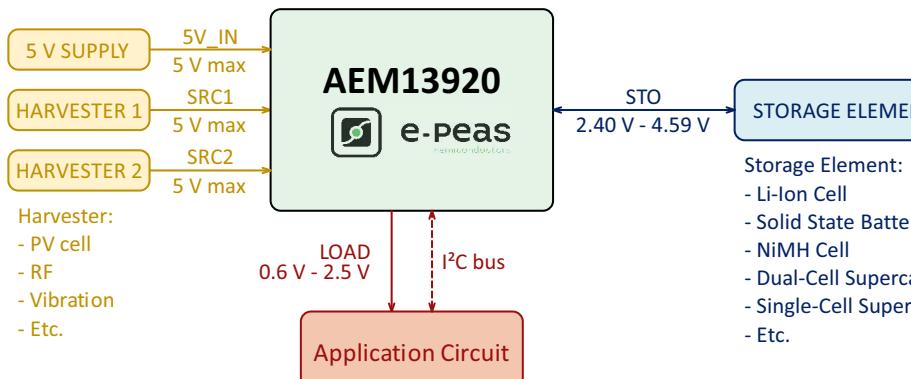


Figure 1: Simplified schematic view

1. Introduction

The AEM13920 is a full-featured energy efficient power management circuit able to harvest energy from two energy sources (connected to [SRC1](#) and/or [SRC2](#)) to supply an application circuit (connected to [LOAD](#)) and use any excess of energy to charge a storage element (connected to [STO](#)). The storage element can also be charged from a 5 V power supply. This is done with a minimal bill of material.

The heart of the AEM13920 is composed of two switching boost converters for energy harvesting and a buck converter for supplying the load. Both have high power conversion efficiency.

The AEM13920 can be configured either by configuration pins or by a set of registers accessed through an I²C bus. Furthermore, some advanced configurations are accessible only through the I²C registers.

A 5 V power input [5V_IN](#) allows for charging the storage element. This is done using a CC/CV (constant current / constant voltage) method. The CC phase maximum current can be configured between 13.5 mA and 135 mA with an external resistor.

At first start-up, as soon as a required cold-start voltage of 275 mV and a sparse amount of power of at least 1.5 μ W is available at [SRCx](#) ([SRC1](#) or [SRC2](#)), the AEM13920 coldstarts. After the cold start, the AEM13920 extracts the power available from the source if the working input voltage is above $V_{SRCx,REG}$ (constant voltage mode) or V_{MPP} (MPPT mode). Cold start can also be done from the 5 V power supply input [5V_IN](#).

The storage element protection levels are configured through three configuration pins ([STO_CFG\[2:0\]](#)), from which the user can select a specific operating mode out of 8 modes that cover most application requirements without any dedicated external component. If none of those 8 modes fit the user's storage element, the voltage thresholds can also be configured individually through I²C registers to allow the user to define a mode with custom specifications.

The [ST_STO](#) status pin provides information about the voltage level of the storage element, and thus about its readiness to supply an application.

Both [SRCx](#) inputs of the AEM13920 can work in Maximum Power Point tracking mode (MPPT) or as constant voltage mode. Those modes are configured with a dedicated pin [SRCx_MODE](#) or through the I²C registers.

When in MPPT mode, the Maximum Power Point (MPP) ratio is configurable thanks to three configuration pins ([SRCx_CFG\[2:0\]](#)) and ensures an optimum biasing of the harvester to maximize power extraction. Depending on the harvester, it is possible to adapt the timings of the MPP evaluations with the two configuration pins ([SRCx_CFG\[4:3\]](#)) that sets the periodicity and the duration of the MPP evaluation. The MPP ratio and the MPP timings can also be configured through the I²C registers.

When in constant voltage mode, the source regulation voltage $V_{SRCx,REG}$ can be configured thanks to four configuration pins ([SRCx_CFG\[4:0\]](#)). The constant voltage can also be configured through I²C registers for higher resolution and extended range of values.

If the storage element is sufficiently charged, the buck converter provides a regulated voltage output on the [LOAD](#) pin, allowing for supplying an application circuit. The regulated voltage can be set through the [LOAD_CFG\[2:0\]](#) pins or through the I²C registers.

A shipping mode can be enabled through the [SHIP_MODE](#) pin, disabling the boost converters, the buck converter as well as the 5 V input, thus preventing any charge or discharge of the battery.



2. Pin Configuration and Functions

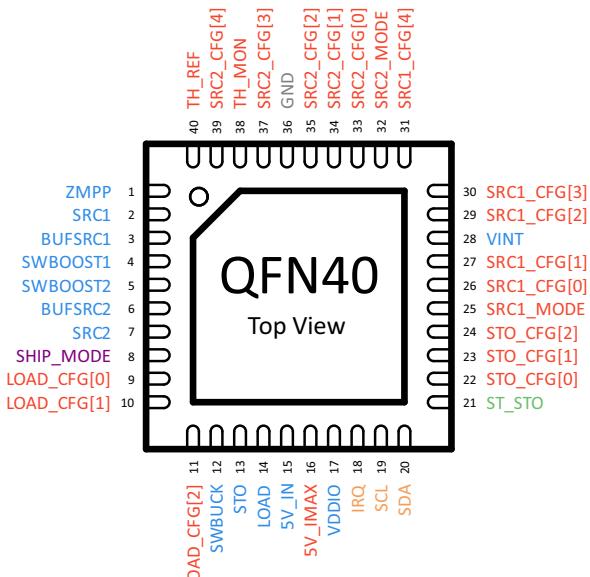


Figure 2: Pinout diagram

NAME	PIN NUMBER	FUNCTION
Power Pins		
SRC1	2	Connection to the energy source harvested by the boost converter #1 and #2 respectively. Connect to GND if not used (typically for single source use of AEM13920).
SRC2	7	
BUFSRC1	3	Connection to an external capacitor buffering the boost converter #1 and #2 inputs respectively. Connect to GND if not used (typically for single source use of AEM13920).
BUFSRC2	6	
SWBOOST1	4	Switching node of the boost converter #1 and #2 respectively. Leave floating if not used (typically for single source use of AEM13920).
SWBOOST2	5	
ZMPP	1	Connection for R_{ZMPP} . Leave floating if not used.
STO	13	Connection to the energy storage element (rechargeable battery).
SWBUCK	12	Switching node of the buck converter. If not used: <ul style="list-style-type: none">- Disable buck converter through LOAD_CFG[2:0] pins or BUCKCFG.VOUT register field.- Leave the SWBUCK pin floating.
LOAD	14	Output voltage of the buck converter to supply an application circuit. If not used: <ul style="list-style-type: none">- Disable buck converter through LOAD_CFG[2:0] pins or BUCKCFG.VOUT register field.- Leave the LOAD pin floating.
5V_IN	15	Input of the 5 V DC power supply. Leave floating if not used.
VDDIO	17	Supply and voltage reference for the I ² C interface, as well as for the IRQ and ST_STO pins. <ul style="list-style-type: none">- If used, connect to a DC power supply.- If not used, connect to GND.
VINT	28	Connection for C_{INT} buffering capacitor. AEM13920 internal power supply (do not connect any external circuit on VINT).

Table 1: Pins description (part 1)



NAME	PIN NUMBER	LOGIC LEVEL		FUNCTION
		LOW	HIGH	
Control Pin				
SHIP_MODE	8	GND	STO	<p>Logic input. When HIGH:</p> <ul style="list-style-type: none"> - Minimum consumption from the storage element. - Storage element charge is disabled (Boost converters are disabled). - Buck (LOAD) is disabled. - Only VINT is charged if energy is available on SRC1 or SRC2. <p>Read as LOW if left floating.</p>
Configuration Pins				
SRC1_MODE	25	GND	VINT	<p>Sets SRCx voltage regulation strategy:</p> <ul style="list-style-type: none"> - LOW: constant voltage mode. - HIGH: MPPT mode (ratio or ZMPP). <p>Read as HIGH if left floating.</p>
SRC2_MODE	32	GND	VINT	
SRC1_CFG[4:0]	SRC1_CFG[4]	31	GND	VINT
	SRC1_CFG[3]	30	GND	VINT
	SRC1_CFG[2]	29	GND	VINT
	SRC1_CFG[1]	27	GND	VINT
	SRC1_CFG[0]	26	GND	VINT
SRC2_CFG[4:0]	SRC2_CFG[4]	39	GND	VINT
	SRC2_CFG[3]	37	GND	VINT
	SRC2_CFG[2]	35	GND	VINT
	SRC2_CFG[1]	34	GND	VINT
	SRC2_CFG[0]	33	GND	VINT
STO_CFG[2]	24	GND	VINT	<p>Used to configure the storage element voltage thresholds.</p> <p>Read as HIGH if left floating.</p>
STO_CFG[1]	23	GND	VINT	
STO_CFG[0]	22	GND	VINT	
LOAD_CFG[2]	11	GND	VINT	<p>Used to configure the LOAD output regulation voltage.</p> <p>Read as HIGH if left floating.</p>
LOAD_CFG[1]	10	GND	VINT	
LOAD_CFG[0]	9	GND	VINT	
5V_IMAX	16	Analog Pin		<p>Connection to an external resistor to set the charging current from the 5V_IN supply to STO.</p> <p>Leave floating if the 5V_IN power supply is not used.</p>
TH_REF	40	Analog Pin		<p>Reference voltage for thermal monitoring.</p> <p>Leave floating if not used.</p>
TH_MON	38	Analog Pin		<p>Connection for thermistor voltage divider mid-point.</p> <p>Connect to VINT if not used.</p>

Table 2: Pins description (part 2)



NAME	PIN NUMBER	LOGIC LEVEL		FUNCTION
		LOW	HIGH	
I²C Pins				
SCL	19	GND	VDDIO	Unidirectional serial clock for I ² C communication. Connect to GND if not used. Connect a pull-up resistor to VDDIO if used. See Section
SDA	20	GND	VDDIO	Bidirectional data line for I ² C communication. Connect to GND if not used.
IRQ	18	GND	VDDIO	Logic output signal to indicate AEM13920 events to external circuit GPIO. Leave floating if not used.
Status Pin				
ST_STO	21	GND	VDDIO	Logic output. - HIGH when in SUPPLY STATE or in SLEEP STATE . - LOW otherwise. Leave floating if not used.
Other pins				
GND	Exposed Pad, 36			Ground connection, each terminal should be strongly tied to the PCB ground plane.

Table 3: Pins description (part 3)



3. Specifications

3.1. Absolute Maximum Ratings

Parameter		Min	Max	Unit
Operating junction temperature T_J		-40	85	°C
Storage temperature T_{stg}		-65	150	°C
Input voltage	<code>SRCx, BUFSRCx, SWBOOSTx, ZMPP, STO, SWBUCK, LOAD, 5V_IN, VDDIO, SHIP_MODE, 5V_IMAX, LOAD_CFG[2:0], SCL, SDA, IRQ, ST_STO.</code>	-0.3	5.50	V
	<code>VINT, SRCx_MODE, SRCx_CFG[4:0], STO_CFG[2:0], TH_REF, TH_MON.</code>	-0.3	2.75	V

Table 4: Absolute maximum ratings

3.2. ESD Ratings

Parameter		Value	Unit
Electrostatic discharge V_{ESD}	Human-Body Model (HBM) ¹	± 2000	V
	Charged-Device Model (CDM) ²	± 1000	V

Table 5: ESD ratings

1. ESD Human-Body Model (HBM) value tested according to JEDEC standard JS-001-2023.

2. ESD Charged-Device Model (CDM) value tested according to JEDEC standard JS-002-2022.

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

3.3. Thermal Resistance

Package	θ_{JA}	θ_{JC}	Unit
QFN-40	50	5	°C/W

Table 6: Thermal data



3.4. Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power conversion						
$P_{SRCx,CS}$	Minimum source power required for cold start.		1.5 ¹			μW
$V_{SRCx,CS}$	Minimum source voltage required for cold start.		0.275			V
V_{MPP}	Target regulation voltage on $SRCx$ when extracting power.	$SRCx_MODE = HIGH$.	0.120			V
$V_{SRCx,REG}$	Target regulation voltage of the source, depending on $SRCx_CFG[4:0]$ configuration or I ² C register.	$SRCx_MODE = LOW$, configured by $SRCx_CFG[4:0]$ pins.	0.143		min (2.104, V_{STO}) ²	V
		$SRCx_MODE = LOW$, configured by I ² C register.	0.120		min (4.455, V_{STO}) ²	V
V_{OC}	Open-circuit voltage of the source.		0.00 ³		5.00	V
V_{5V_IN}	Voltage on the $5V_IN$ pin to allow for charging the battery.		3.50 ⁴		5.50	V
$P_{5V_IN,MIN}$	Minimum power on $5V_IN$ to start charging the battery.	$V_{5V_IN} = 3.50\text{ V}$		51		μW
		$V_{5V_IN} = 5.50\text{ V}$		80		
$I_{5V,CC}$	Maximum charging current of 5 V charger when in constant current (CC) mode. This is programmed by the resistor on the $5V_IMAX$ pin.		13.50		135	mA
V_{VDDIO}	Voltage on $VDDIO$.		1.50		5.00	V
Timing						
$T_{MPPT,SAMPLING}$	Open-circuit duration for the MPP evaluations (see Table 12).	Configured by $SRCx_CFG[4:0]$.	2		256	ms
		Configured by I ² C.			512	
$T_{MPPT,PERIOD}$	Time between two MPP evaluations (see Table 12).	Configured by $SRCx_CFG[4:0]$.	0.128		16.38	s
		Configured by I ² C.				
T_{CRIT}	In SUPPLY STATE , the AEM13920 waits for T_{CRIT} before switching to OVDIS STATE when V_{STO} drops below V_{OVDIS} .			2.50		s
$T_{GPIO,MON}$	GPIO reading rate.			2.05		s
$T_{TEMP,MON}$	Temperature monitoring rate.			8.19		s
$T_{5V,RISE}$	Minimum rise time from 0 V to 5 V on the $5V_IN$ pin (see Section 6.8).			50		μs

Table 7: Electrical characteristics (part 1)

1. For $V_{SRCx} = 0.275\text{ V}$. Cold-start duration is typically 3 minutes.
2. The maximum value of $V_{SRCx,REG}$ is determined by the highest configurable voltage for $V_{SRCx,REG}$ but it must never be higher than the storage element voltage (V_{STO}) to ensure proper operation.
3. When the open-circuit voltage is below the source regulation voltage (MPPT or constant voltage), the AEM13920 does not extract power from the source. Voltages down to **GND** voltage does not damage the AEM13920 though.
4. For the 5 V charger to operate, the voltage on $5V_IN$ must be greater than or equal to 3.5 V and at least 200 mV higher than the voltage on **STO**.



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Storage element						
V_{STO}	Voltage on the storage element.		2.40 ¹		4.59 ²	V
V_{OVDIS}	Minimum voltage accepted on the storage element before stopping to supply LOAD (see Section 6.4).	Configured by STO_CFG[2:0] .	2.50		3.50	V
		Configured by I ² C (with 18 mV steps).	2.40		3.58	V
V_{CHRDY}	Minimum voltage accepted on the storage element before starting to supply LOAD in START STATE (see Section 6.4).	Configured by STO_CFG[2:0] .	2.55		3.55	V
		Configured by I ² C (with 18 mV steps).	2.46		3.64	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging (see Section 6.4).	Configured by STO_CFG[2:0] .	3.50		4.12	V
		Configured by I ² C (with 18 mV steps).	2.70		4.59	V
Internal supply & quiescent current						
V_{INT}	Internal voltage supply.		2.20	2.25	2.30	V
$V_{INT,RESET}$	Minimum voltage on VINT before switching to RESET STATE (from any other state).			2.0		V
$V_{INT,CS}$	Minimum voltage on VINT to allow the AEM13920 to switch from RESET STATE to SENSE STO STATE .			2.3		V
$I_{QSUPPLY}$	Quiescent current on STO in SUPPLY STATE . ³	Buck enabled (LOAD).		645		nA
		Buck disabled (LOAD).		460		nA
I_{QSLEEP}	Quiescent current on STO in SLEEP STATE . ³	Buck enabled (LOAD).		435		nA
		Buck disabled (LOAD).		275		nA
$I_{QSHIP,SRCx}$	Quiescent current on STO when the shipping mode functionality is enabled (SHIP_MODE set HIGH).	Energy on SRCx .				
I_{QSHIP}		No energy on SRCx .	10			nA
I_{QOFF}	Quiescent current on STO when the AEM13920 is in RESET STATE .					

Table 8: Electrical characteristics (part 2)

1. As set by the battery overdischarge threshold configuration.

2. As set by the battery overcharge threshold configuration.

3. Both boost converters are enabled but not extracting current from **SRCx**. The **LOAD** pin is left floating.



3.5. Recommended Operation Conditions

Symbol	Parameter	Min ¹	Typ	Max ¹	Unit	
External components						
L_{BOOSTx}	Inductor of the boost converters (optional ²).	3.3 ³	33		μH	
C_{SRCx}	Capacitor decoupling the $BUFSRCx$ pin (optional ²).	3.3 ⁴		10^5	μF	
L_{BUCK}	Inductor of the buck converter (optional ⁶).	1.7 ³	10		μH	
C_{LOAD}	Capacitor of the buck converter (optional ⁶).	10	22		μF	
C_{INT}	Capacitor decoupling the $VINT$ terminal (mandatory).	5	10		μF	
C_{STO}	Capacitor decoupling the STO terminal (mandatory).	5	10		μF	
C_{5V}	Capacitor decoupling the $5V_IN$ terminal (optional ⁷).	22	47		μF	
R_{5V_IMAX}	Resistor for configuring the 5V charger current when in constant current (CC) mode (optional ⁷).	0.37		3.7	$k\Omega$	
R_{SDA}	Pull-up resistors for the I ² C interface (optional ⁸).		1		$k\Omega$	
R_{SCL}						
R_{TH}	NTC thermistor used for thermal monitoring operation (optional ⁹).	R0	0	10^{10}	250	$k\Omega$
		Beta		3380^{10}		K
R_{DIV}	Resistor used to create a resistive divider with R_{TH} for thermal monitoring operation (optional ⁹).	4	22^{10}	40	$k\Omega$	
R_{ZMPP}	Resistor used for the configuration of the ZMPP function (optional ¹¹).	33		1M	Ω	

Table 9: Recommended external components

1. All minimum and maximum values are real components values, taking into account tolerances, derating, temperatures, voltages and any operating conditions (special care must be taken with capacitor derating).
2. Mount only if boost converter x is used.
3. Those minimum values are only applicable with minimum timings (see Sections 9.5 and 9.6).
4. This value may be reduced if the peak current in L_{BOOSTx} is low enough to not cause excessive ripple on $BUFSRCx$. The L_{BOOSTx} peak current depends on the combination of boost x timing and L_{BOOSTx} inductance. To maintain maximum efficiency, the guideline is to keep-the-peak to peak ripple below 10% of the source target regulation voltage.
5. Typically, a 22 μF / 10 V (MLCC, 0603) capacitor can be used as the capacitance DC bias derating lowers the effective capacitance down to $\sim 5 \mu F$ at 5 V.
6. Mount only if buck converter is used.
7. Mount only if the 5 V charger is used.
8. Mount only if the I²C interface is used. For more information on how to select the value of these resistors, refer to “Pull-up resistor sizing” section in NXP’s UM10204 “I²C-bus specification and user manual”.
9. Mount only if the temperature monitoring feature is used.
10. Those values allow for having a default setting at startup of -25 °C for the “cold” threshold and +70 °C for the “hot” threshold, for both charging and discharging.
11. Mount only if the ZMPP feature is used.



Symbol	Parameter		
Logic input pins			
SRCx_MODE	Boost source voltage regulation mode.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
SRCx_CFG[4:0]	Boost source voltage regulation settings.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
STO_CFG[2:0]	Storage element voltage thresholds configuration.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
LOAD_CFG[2:0]	Configuration of the LOAD buck output voltage regulation.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
SHIP_MODE	Shipping mode enable pin.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to STO.
I²C interface pins			
SCL	I ² C clock signal pin.	Pull-up to VDDIO with resistors R_{SCL} and R_{SDA} .	
SDA	I ² C data signal pin.		

Table 10: Logic input pins and I²C interface pins connections



3.6. Typical Characteristics

3.6.1. Boost Converter Conversion Efficiency

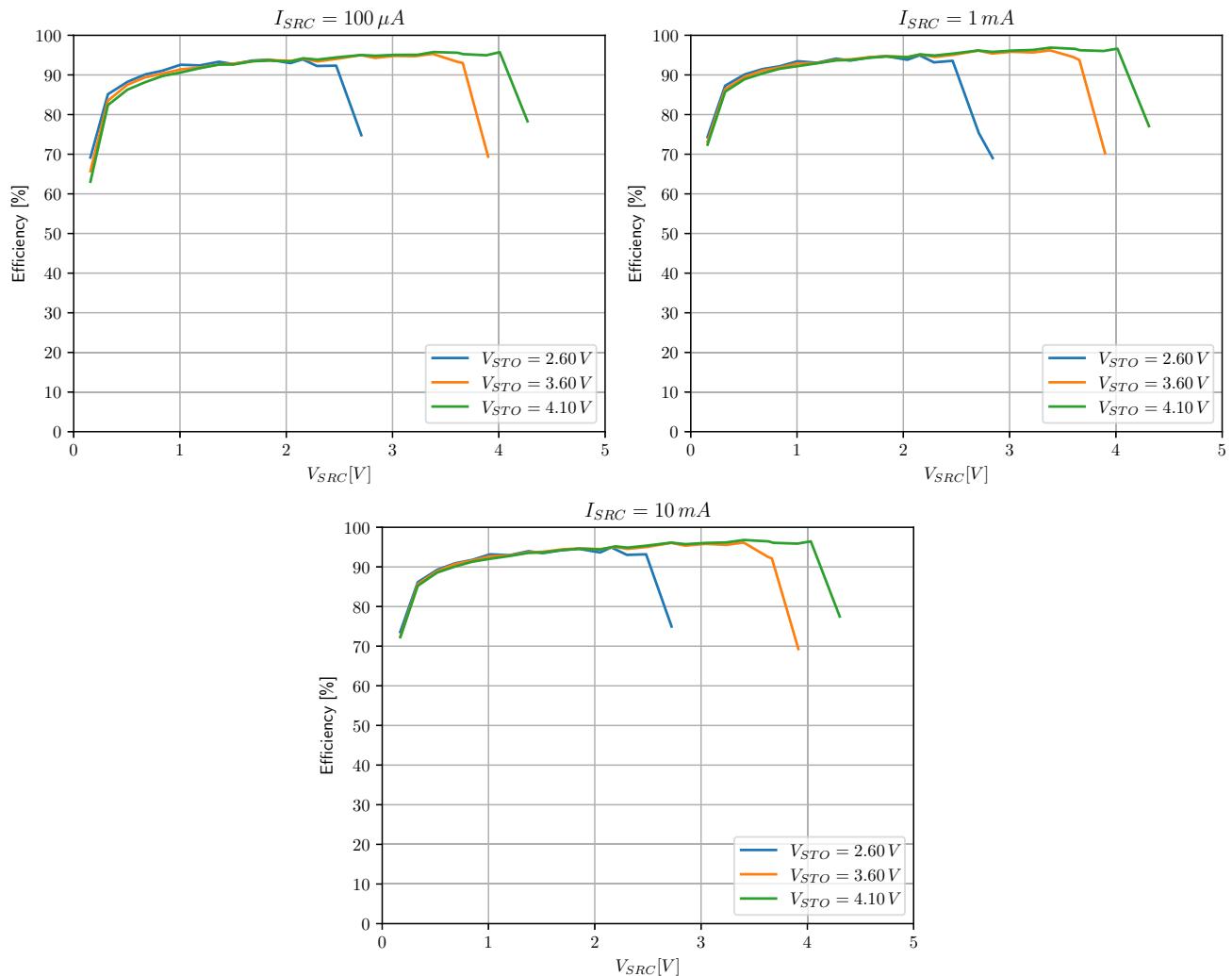


Figure 3: Boost converter efficiency with $L_{BOOSTx} = 33 \mu H$ (Coilcraft LPS4018-333MRB), $BSTxCFG.TMULT = 0x02$ (x3)

NOTE: The boost efficiency data presented in Figure 3 include the AEM13920 quiescent current.



3.6.2. Buck Converter Conversion Efficiency

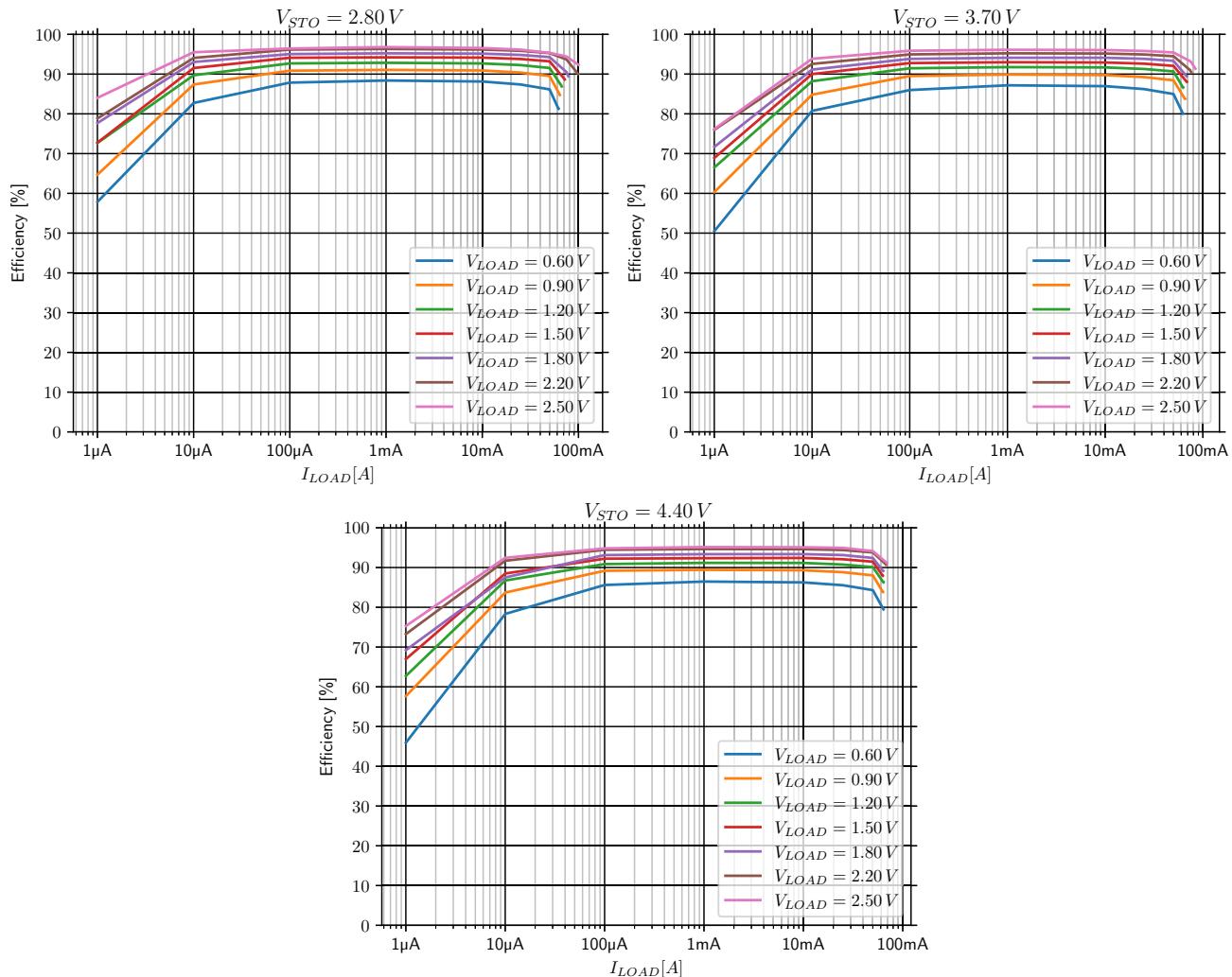


Figure 4: Buck (LOAD) converter efficiency with $L_{BUCK} = 10 \mu H$ (Coilcraft LPS4018-103MRB), $BUCKCFG.TMULT = 0x01$ (x2)

NOTE: The quiescent current of the AEM13920 is not included in the buck efficiency data presented in Figure 4, as it has already been included in the boost efficiency data shown in Section 3.6.1. This quiescent current has been measured with the boost converter in **SLEEP STATE** and the buck converter switched off.



4. Functional Block Diagram

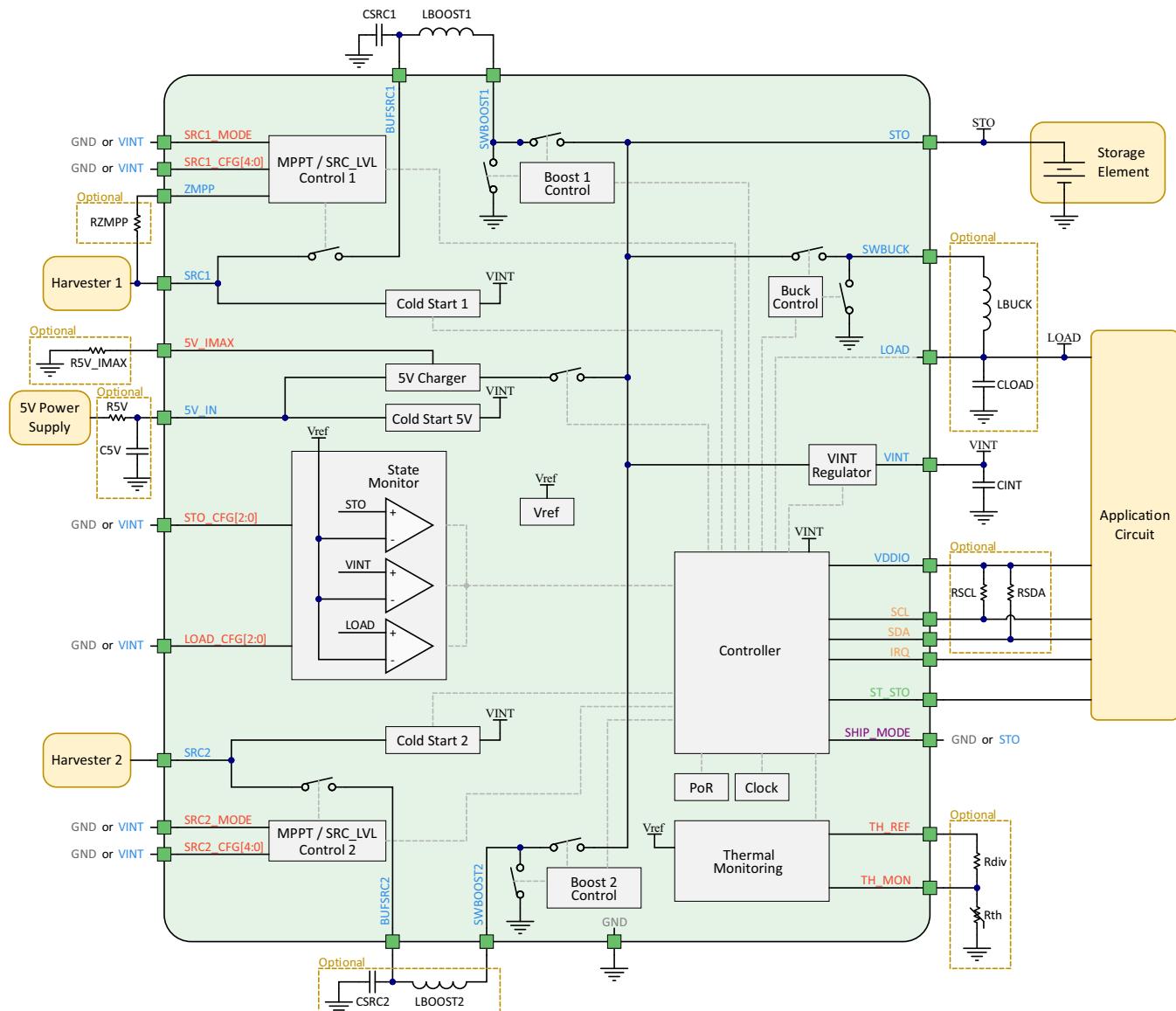


Figure 5: Functional block diagram



5. Theory of Operation

5.1. Cold-Start Circuits

The AEM13920 is able to coldstart from either $SRCx$ or from $5V_{IN}$ (see Table 7 for cold-start conditions). The cold-start circuit supplies the AEM13920 internal circuit (connected to $VINT$) when the device is in **RESET STATE**, **SENSE STO STATE** or **OVDIS STATE**.

See Table 7 for the typical AEM13920 minimum cold-start voltage $V_{SRCx,CS}$ and minimum cold-start power $P_{SRCx,CS}$. Those results have been measured starting with all AEM13920 nodes discharged, except V_{STO} that is charged above V_{CHRDY} . The cold start is considered to be finished when $LOAD$ is supplied (buck is enabled), meaning that the AEM13920 has switched to **SUPPLY STATE**.

5.2. Boost Converters

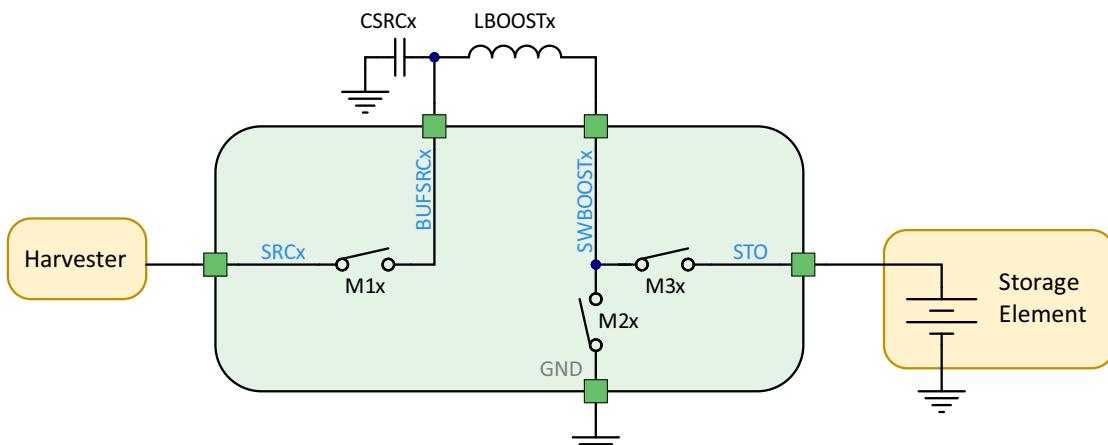


Figure 6: Simplified schematic view of the boost converters

Please note that the following explanations apply to both boost converters #1 and #2.

5.2.1. Operation Principle

The boost (step-up) converter raises the voltage available at $BUFSRCx$ to a level suitable for charging the storage element, in the range of 2.40 V to 4.59 V, according to the system configuration. The switching transistors of the boost converter are $M2x$ and $M3x$. The reactive power component of this converter is the external inductor L_{BOOSTx} .

$M1x$ allows for disconnecting the $SRCx$ pin from $BUFSRCx$, which happens in the following cases:

- When measuring the source open-circuit voltage, if source mode is MPPT (see Section 5.2.2).

- When the boost converter is disabled through I²C (see Section 9.5).
- When AEM13920 is in **SLEEP STATE**, **SENSE STO STATE** or **RESET STATE** (see Section 5.9).
- When temperature is out of range (see Section 5.4).
- When a suitable power supply is connected to the $5V_{IN}$ pin (both boosts are disabled in that case).

When the boost converter is extracting energy from the source, $M1x$ is closed, connecting $SRCx$ to $BUFSRCx$.



Target source regulation voltage can be determined by:

- The MPPT module when **SRCx_MODE** is HIGH (ratio of open-circuit voltage or target impedance connected to **ZMPP** (see Section 5.2.2).
- The constant voltage regulation setting when **SRCx_MODE** is LOW (see Section 5.2.3).

BUFSRCx is decoupled by the capacitor **C_{SRCx}**, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the **STO** pin, which voltage is **V_{STO}**. This node is linked to the output of the boost converter through transistor M3x. When energy harvesting is occurring, the boost converter charges the battery.

The maximum current supplied to the **STO** pin depends on both the value of **L_{BOOSTx}** and the boost converters timings for charging and discharging **L_{BOOSTx}**, and thus, its peak current **I_{BOOST,PEAK}**. The boost timings can be configured thanks to the I²C register field **BSTxCFG[4:2]**. See Section 6.5 for default boost timing values and Section 9.5 for further information, as well as typical combinations of **L_{BOOSTx}** inductor value and boost converters timings.

While using an energy source is mandatory, using both boost converters is not: user might use a single boost converter or even use the AEM13920 only with the 5 V charger as energy source. The following connections must be done if a boost converter is not used:

- **SRCx** and **BUFSRCx** to GND.
- Leave **SWBOOSTx** floating.

5.2.2. Maximum Power Point Tracking

This section describes the AEM13920 behavior when source regulation mode is MPPT. Switching to this mode is done by setting the **SRCx_MODE** pin HIGH or by setting **SRCxREGU0.MODE** I²C register field bit HIGH (see Sections 6.2 and 9.3).

The MPPT module is active during **START STATE**, **OVDIS STATE** and **SUPPLY STATE**.

5.2.2.1. Open-Circuit Voltage Ratio

In open-circuit voltage ratio mode, the AEM13920 MPPT relies on the fact that, for several models of harvesters (typ. solar cells), the ratio between the maximum power point voltage (**V_{MPP}**) and the open-circuit voltage (**V_{OC}**) is constant for a wide range of harvesting conditions. For a solar cell, that means that **V_{MPP} / V_{OC}** is constant for any lighting conditions, even though both voltages increase when luminosity increases. Please note that this is valid for a large variety of harvesters, not only solar cells.

The Maximum Power Point (MPP) ratio **V_{MPP} / V_{OC}** differs from one harvester model to another. User must set the MPP ratio to match the specifications of the harvester model used and thus maximize power extraction. This ratio is set with the configuration pins **SRCx_CFG[2:0]** (see Section 6.2) or with the I²C interface register field **SRCxREGU0.CFG0** (see Section 9.3).

The MPPT module evaluates the open-circuit voltage **V_{OC}** periodically to ensure optimal power extraction at any time. The sampling period **T_{MPPT,PERIOD}** and sampling duration **T_{MPPT,SAMPLING}** of the evaluation of **V_{OC}** are set with the configuration pins **SRCx_CFG[4:3]** (see Section 6.2) or by configuring fields from the **SRCxREGU1** register (see Section 9.3).

Every **T_{MPPT,PERIOD}**, the MPPT stops extracting power from the source, waits during **T_{MPPT,SAMPLING}** for the source to rise to its open-circuit voltage **V_{OC}**, and measures **V_{OC}**. The AEM13920 allows for a wide range of **V_{MPP}** levels, and offers a choice of eight values for the **V_{MPP} / V_{OC}** ratio.

5.2.2.2. ZMPP

Some harvesters provide better performance when connected to a circuit with constant input resistance. The AEM13920 boost converter #1 MPPT can be set as constant input resistance by enabling the ZMPP function. This can be done by setting all **SRC1_CFG[2:0]** pins HIGH (see Section 6.2) or by setting the field **SRC1REGU0.CFG0** to 0x07 (see Section 9.3).

In ZMPP mode, the AEM13920 regulates the input resistance of **SRC1** to match the resistance **R_{ZMPP}** connected to the **ZMPP** pin. Operation is similar to that of the **V_{MPP} / V_{OC}** mechanism described in Section 5.2.2.1:

- Every **T_{MPPT,PERIOD}**, the AEM13920 disconnects **SRC1** from **BUFSRC1**, and connects the **ZMPP** pin to GND, with **R_{ZMPP}** thus becoming the source load resistance.
- After a **T_{MPPT,SAMPLING}** delay, the AEM13920 measures the voltage on **SRC1**, loaded by **R_{ZMPP}**. The measured voltage is the new **SRC1** input regulation voltage.

When in ZMPP mode, **T_{MPPT,SAMPLING}** is determined as for the **V_{MPP} / V_{OC}** mode: either by **SRC1_CFG[4:3]** (see Section 6.2) or by the **SRC1REGU1.CFG1** I²C register field (see Section 9.3).

Please note that the ZMPP feature is only available on boost converter 1, or when a harvester is connected on both boost converters simultaneously, as described in Section 5.2.5.

5.2.3. Source Constant Voltage Regulation

This section describes the AEM13920 behavior when source regulation mode is constant voltage. Switching to this mode is done by setting the **SRCx_MODE** LOW or by setting **SRCxREGU0.MODE** I²C register field bit LOW (see Sections 6.3 and 9.3).



During **START STATE**, **OVDIS STATE** and **SUPPLY STATE**, the voltage on **SRCx** is regulated to a voltage configured by the user. The AEM13920 offers a wide choice of values for the source regulation voltage $V_{SRCx,REG}$ (see Section 6.3).

In constant voltage regulation mode, the AEM13920 behaves as follows:

- If the open-circuit voltage V_{OC} of the harvester is lower than $V_{SRCx,REG}$, the AEM13920 does not extract power from the source.
- If **SRCx** voltage is higher than V_{OC} , the AEM13920 regulates V_{SRCx} to $V_{SRCx,REG}$ and thus, extracts power from the source.
- If $V_{SRCx,REG}$ is configured by I²C below V_{SRCLOW} thanks to the SRCxREGUX.LVL register, the AEM13920 enters **SLEEP STATE** (see Section 5.9.6 and Section 9.3.3).

5.2.4. Automatic High-Power Mode

When the AEM13920 detects that the energy available on **SRCx** is high enough, the boost converter automatically switches to high-power mode.

Preventing the AEM13920 to switch to high-power mode may allow to use an inductor with half peak current rating for L_{BOOSTx} (see Section 9.5). On the other hand, allowing the AEM13920 to switch to high-power mode increases the maximum current that the AEM13920 can harvest from **SRCx** to **STO**.

Automatic high-power mode is enabled by default and can be disabled by setting the BSTxCFG.ENHP register bit to 0 through the I²C interface.

5.2.5. Using Both Boost Converters in Parallel

It is possible to use the two boost converters in parallel to double the current that can be extracted from a single harvester.

To do so, user must configure the AEM13920 as follows:

- Connect the harvester simultaneously on **SRC1** and **SRC2**.

- Configure both boost converters input with identical regulation settings (MPPT with the same ratio or same constant voltage).
- C_{SRC1} , C_{SRC2} , L_{BOOST1} and L_{BOOST2} must all be populated and both boost timings must be configured accordingly.

Please note that ZMPP can be configured to work with interconnected sources. in this case, the AEM13920 must be configured as shown in Figure 7:

- **SRC1** and **SRC2** as MPPT (**SRC1_MODE** and **SRC2_MODE** HIGH).
- **SRC1** MPP ratio to ZMPP.
- **SRC2** MPP ratio to 100%.
- A single R_{ZMPP} resistor connected between **ZMPP** and **SRC1/SRC2**.

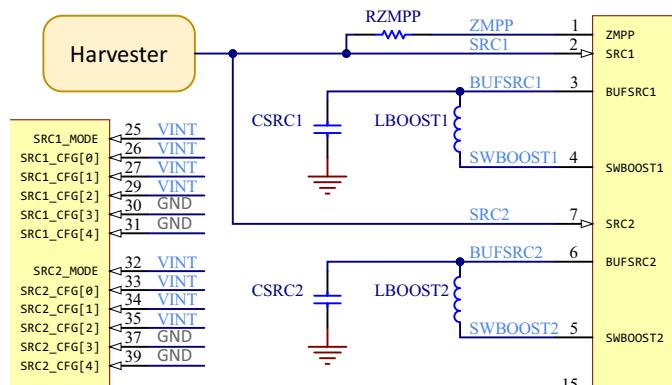


Figure 7: ZMPP connection with both boost converters used in parallel

See Section 5.2.2.2 for further information about ZMPP.



5.3. Buck Converter

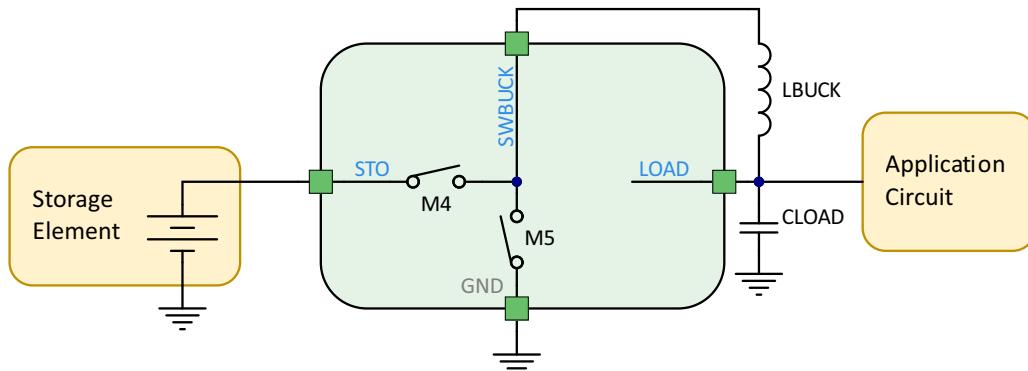


Figure 8: Simplified schematic view of the buck converter

The buck (step-down) converter transfers energy from the battery connected on **STO** to the regulated **LOAD** output. The switching transistors of the buck converter are M4 and M5. The reactive power component of this converter is the external inductor **L_{BUCK}**. **LOAD** is decoupled by the capacitor **C_{LOAD}**, which smooths the voltage against the current pulses induced by the consumption of the external circuit connected to **LOAD**.

Setting the **LOAD** regulation voltage **V_{LOAD}** or disabling the buck converter is done through **LOAD_CFG[2:0]** pins (see Sections 6.6) or I²C register BUCKCFG (see Section 9.6).

After cold start and if enabled, the buck converter starts once **V_{STO}** is higher than **V_{CHRDY}**. It stays enabled, and thus, regulates **V_{LOAD}** until **V_{STO}** drops below **V_{OVDIS}**.

The maximum current supplied to the **LOAD** pin depends on both the value of **L_{BUCK}** and the buck converter timings for charging and discharging **L_{BUCK}**, and thus, its peak current **I_{BUCK,PEAK}**. The buck timings can be configured thanks to the I²C register field BUCKCFG[5:3]. See Section 6.6.2 for default buck timing values and Section 9.6 for further information and typical combinations of **L_{BUCK}** inductor value and buck converter timings.

Using the buck converter is not mandatory. If not used, user must do the following:

- Connect all **LOAD_CFG[2:0]** to GND (LOW) to disable the buck converter.
- Leave **SWBUCK** and **LOAD** floating.

When the difference between **V_{STO}** and **V_{LOAD}** is too small for the buck converter to keep working properly, it switches to "bang-bang" controlled converter mode:

- When **V_{LOAD}** is too low, a switch connects **STO** directly to **LOAD**, making **V_{LOAD}** rise.
- When **V_{LOAD}** is too high, the controller disconnects **STO** and **LOAD** so that **V_{LOAD}** decreases.

This happens when the following condition is satisfied:

$$V_{STO} - V_{LOAD} < 0.25V$$

In that case, efficiency is lower than in buck mode.



5.4. Thermal Monitoring

Thermal monitoring allows for protecting the storage element. Enabling this functionality requires the use of a resistor (R_{DIV}) and a NTC thermistor (R_{TH}), forming a resistive divider. See Figure 10 for connections of those external components. The TH_REF terminal allows for applying a reference voltage to the resistive divider while TH_MON is the measuring point. The temperature evaluation is done periodically every $T_{TEMP,MON}$ (see Table 7). To spare power, the divider is biased only during this evaluation. See Section 6.7 for further information about thermal monitoring configuration.

Thermal monitoring is optional, if not used connect TH_MON to $VINT$ and leave TH_REF floating.

5.5. Average Power Monitoring

The Average Power Monitoring (APM) module allows for evaluating the energy transfer from $SRCx$ to STO .

5.6. IRQ Pin

The IRQ pin allows the application circuit to be notified of various events occurring in the AEM13920 (rising edge on the IRQ pin). At startup, the only event that is enabled is $I2CRDY$, signaling that the AEM13920 has finished to coldstart and thus, that it is out from **RESET STATE**. Other events can be enabled by writing the $IRQENO$ and $IRQEN1$ registers (see Section 9.11).

When the IRQ pin shows a rising edge, the event that triggered it can be determined by reading the $IRQFLG0$ and $IRQFLG1$ registers (see Section 9.12). IRQ pin is reset when the corresponding $IRQFLGx$ register is read.

5.7. 5 V Charger

The AEM13920 is equipped with a 5 V charger for fast charging of the battery connected on the STO pin.

The 5 V charger can be used when the following conditions are met:

- $V_{5V_IN} \geq 3.5$ V.
- $V_{5V_IN} \geq V_{STO} + 200$ mV.

With the 5 V charger, the battery is charged by implementing a constant current / constant voltage operation (CC/CV):

- Constant current (CC) operation:
 - When $V_{STO} < V_{OVCH} - 50$ mV.
 - Battery charging current $I_{5V,CC}$ is configured by the value of the R_{5V_IMAX} resistor connected to the $5V_IMAX$ pin (see Section 6.8 for further details about R_{5V_IMAX} configuration). $I_{5V,CC}$ range is from 13.5 mA to 135 mA.
- Constant voltage (CV) operation:
 - When $V_{OVCH} - 50$ mV $< V_{STO} < V_{OVCH}$.
 - The charging current $I_{5V,CV}$ gradually decreases to zero as V_{STO} reaches V_{OVCH} .

Using the 5 V charger is not mandatory. When not used, leave both $5V_IN$ and $5V_IMAX$ pins floating.

5.8. Shipping Mode

The shipping mode feature allows for forcing the AEM13920 in **RESET STATE** (see Figure 9 and Section 5.9.1), thus, disabling all AEM13920 functionalities including both boost converters, the buck converter and the 5 V charger. Only $VINT$ is charged if energy is available from $SRCx$. The battery is no longer charged or discharged.

See Section 6.9 for shipping mode enabling and disabling.

5.9. State Machine Description

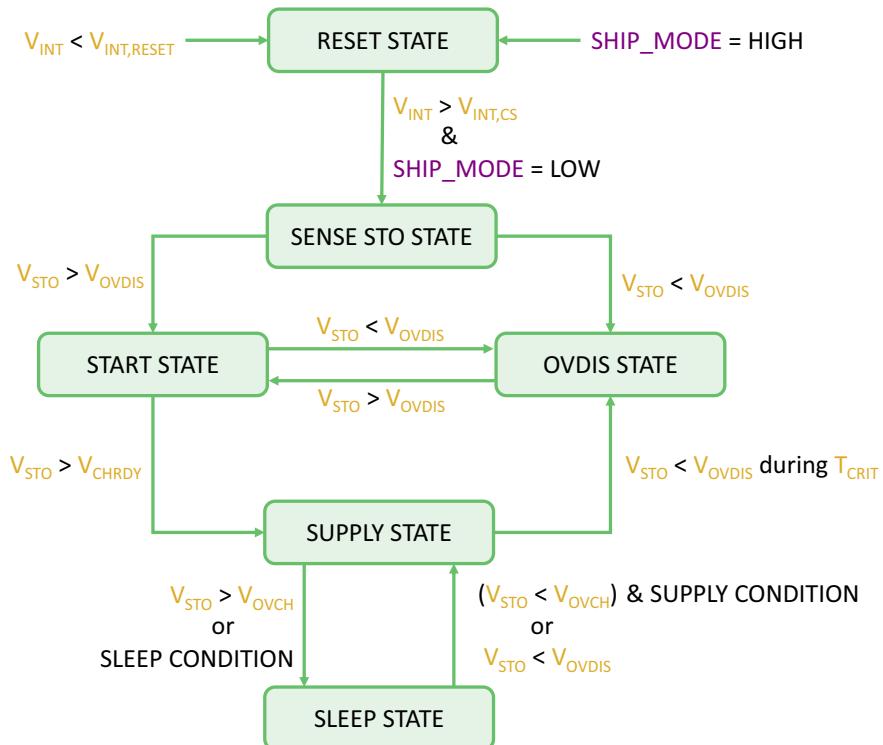


Figure 9: AEM13920 state machine

5.9.1. Reset State

The AEM13920 enters **RESET STATE** if one of the following is true:

- V_{INT} is below $V_{INT,RESET}$ (see Table 8).
- shipping mode is enabled ($SHIP_MODE$ is HIGH).

In **RESET STATE**, the AEM13920 behaves as follows:

- The AEM13920 is performing a cold start to make V_{INT} rise to 2.3 V. Cold start can be done from any of the following energy sources:
 - **SRCx** ($V_{SRCx} > 0.275$ V and $P_{SRCx,CS} > 1.5$ μ W).
 - **5V_IN** ($V_{5V_IN} > 3.5$ V).
- The AEM13920 internal circuit, connected on **VINT**, is supplied by **SRCx** or **5V_IN**. No current is drawn from the battery.
- **ST_STO** is LOW.

The AEM13920 stays in **RESET STATE** until the power available on either **SRCx** meets the cold-start requirements long enough to make V_{INT} reach 2.3 V (see Table 7). Then:

- If shipping mode is disabled ($SHIP_MODE$ is LOW), the AEM13920 reads the value on all configuration pins and switches to **SENSE STO STATE**.

- If shipping mode is enabled ($SHIP_MODE$ is HIGH), the AEM13920 stays in **RESET STATE** until shipping mode is disabled by setting $SHIP_MODE$ LOW. Please note that **SHIP_MODE** is read every $T_{GPIO,MON}$ (about 2 s).

Please note that, from any state, the AEM13920 will switch to **RESET STATE** if V_{INT} drops below $V_{INT,RESET}$.

5.9.2. Sense STO State

In **SENSE STO STATE**, a first measure of V_{STO} is performed by the AEM13920.

- If $V_{STO} > V_{OVDIS}$, the AEM13920 switches to **START STATE**.
- If $V_{STO} < V_{OVDIS}$, the AEM13920 switches to **OVDIS STATE**.
- The AEM13920 internal circuit, connected on **VINT**, is supplied by **SRCx** or **5V_IN**. If not enough power is available on either of those pins, the AEM13920 switches to **RESET STATE**. No current is drawn from the battery.
- **ST_STO** is LOW.
- The levels of **SDA** and **SCL** pins are evaluated to decide whether the I²C should be enabled (see Section 6.1.2)

In **SENSE STO STATE**, none of the DCDC converters are running. This state lasts for about 2 ms.



5.9.3. Start State

When in **SENSE STO STATE**, the AEM13920 switches to **START STATE** if V_{STO} is above V_{OVDIS} .

In **START STATE**, the AEM13920 behaves as follows:

- The battery connected on **STO** is charged by the boost converters or by the 5V charger, until V_{STO} reaches V_{CHRDY} .
- The AEM13920 internal circuit connected on **VINT** is supplied by the battery regardless of the power available on **SRCx** or **5V_IN**.
- The buck converter (**LOAD**) is disabled.
- **ST_STO** is LOW.

5.9.4. Supply State

When in **START STATE**, the AEM13920 switches to **SUPPLY STATE** if V_{STO} is above V_{CHRDY} .

In **SUPPLY STATE**, the AEM13920 behaves the same as when in **START STATE**, but with the following differences:

- The buck converter driving **LOAD** is enabled (if enabled by the user).
- **ST_STO** is HIGH.

When in **SUPPLY STATE**, the AEM13920 switches to **SLEEP STATE** if one of the following conditions is met:

- $V_{STO} > V_{OVCH}$.
- **SLEEP CONDITION** (see Section 5.9.6).

5.9.5. OVDIS State

The AEM13920 switches to **OVDIS STATE** if:

- V_{STO} is below V_{OVDIS} when in **SENSE STO STATE** or **START STATE**.
- V_{STO} remains below V_{OVDIS} for more than T_{CRIT} when in **SUPPLY STATE**.

In **OVDIS STATE**, the AEM13920 behaves as follows:

- The battery connected on **STO** is charged by the boost converters and/or by the 5V charger, until V_{STO} exceeds V_{OVDIS} .
- The AEM13920 internal circuit, connected on **VINT**, is supplied by **SRCx** or **5V_IN**. If not enough power is available on either of those pins, the AEM13920 switches to **RESET STATE**. No current is drawn from the battery.
- The buck converter (**LOAD**) is disabled.
- **ST_STO** is LOW.

5.9.6. Sleep State

SLEEP STATE allows for reducing the AEM13920 internal circuit consumption when none of the **SRCx** provides enough power or when the battery is fully charged. Thus, battery discharging is kept minimal. **SLEEP STATE** is also reached when charging is not allowed (temperature outside range, boost converters disabled, V_{SRCx} below the V_{SRCLOW} threshold).

The following conditions are defined:

- **SLEEP CONDITION** is true if one of the following conditions is true:
 - Temperature outside of the range (see Section 6.7).
 - All boost converters are disabled through I²C (see Section 9.5).
 - Voltage on both **SRCx** is below the V_{SRCLOW} threshold (see Section 9.10).
- **SUPPLY CONDITION** is true if all the following conditions are true:
 - Temperature within the range (see Section 6.7).
 - At least one boost converter is enabled (see Section 9.5).
 - Voltage on one of **SRCx** is above the V_{SRCLOW} threshold (see Section 9.10).

In **SLEEP STATE**, the AEM13920 behaves as follows:

- The battery connected on **STO** is not charged by **SRCx**, allowing for reducing the quiescent current on **VINT** and thus on **STO**.
- If V_{STO} is below V_{OVCH} , the battery connected on **STO** can be charged from the 5V charger by connecting a power source on **5V_IN**.
- The AEM13920 internal circuit connected on **VINT** is supplied by the battery regardless of the power available on **SRCx** or **5V_IN**.
- The buck converter (**LOAD**) is enabled (if enabled by the user).
- **ST_STO** is HIGH.

When in **SLEEP STATE**, the AEM13920 switches back to **SUPPLY STATE** if one of the following conditions is met:

- **SUPPLY CONDITION** and $V_{STO} < V_{OVCH}$.
- $V_{STO} < V_{OVDIS}$.



6. System Configuration

6.1. Configuration Pins and I²C

6.1.1. Configuration Pins

After a cold start, the AEM13920 reads the configuration pins. Those are then read periodically every $T_{GPIO,MON}$. The configuration pins can be changed on-the-fly. The floating configuration pins are read as HIGH, except **SHIP_MODE** which is read as LOW.

NOTE: all the read-only registers (with addresses from IRQFLG0/0x15) can be read and contain valid data even if the AEM13920 is configured through the GPIO. The only exception is the APM-related registers that are no longer updated when using the GPIO configuration.

6.1.2. Configuration by I²C

To configure the AEM13920 through the I²C interface after a cold start, user must wait for the **IRQ** pin to rise, showing that the AEM13920 is out of **RESET STATE** and is ready to communicate with I²C. Please note that the **IRQ** pin is always low during **RESET STATE**. See Section 5.6 for further informations about the **IRQ** pin.

Once the above procedure is done, user can then write to the desired registers and validate the configuration by setting the CTRL.UPDATE register field. All configuration pins are then ignored (except the **SHIP_MODE** pin) and all configurations are set by the register values. All registers have a default value, that can be found in Table 17.

Registers are stored in a volatile memory, so their value is lost when **VINT** drops below the reset voltage $V_{INT,RESET}$, making the AEM13920 switch to **RESET STATE**. **VDDIO** is only for I²C communication bus supply, so register values are kept whether **VDDIO** is supplied or not once registers are written.

*NOTE: It is important to note that if both **SDA** and **SCL** pins are read LOW (**GND**) during **SENSE STO STATE**, the I²C interface will be disabled. In this case, the **IRQ** pin will remain LOW, even if the AEM13920 is out of **RESET STATE**. To enable the I²C after this point, the master must first send an I²C message (**START + DATA**) to the AEM13920, such as the address of the AEM13920. Once the I²C interface is enabled, **IRQ** pin is set HIGH to indicate that the I²C interface is ready (**IRQFLG0.I2CRDY**).*

6.2. Maximum Power Point Tracking

The following configurations apply when **SRCx_MODE** is HIGH, so that the boost converter is in MPPT mode. When configuring the MPPT module, user can set the MPP ratio and the timings, as shown in Tables 11 and 12.

Configuration pins			MPPT Ratio [%]
SRCx_CFG[2:0]			R_{MPPT}
L	L	L	35%
L	L	H	50%
L	H	L	65%
L	H	H	70%
H	L	L	75%
H	L	H	80%
H	H	L	85%
H	H	H	ZMPP (SRC1) / 100% (SRC2)

Table 11: MPPT ratio configuration with SRCx_CFG[2:0] pins

Configuration pins		Sampling Duration [ms]	Period [ms]
SRCx_CFG[4:3]		$T_{MPPT,SAMPLING}$	$T_{MPPT,PERIOD}$
L	L	2	128
L	H	8	512
H	L	32	2048
H	H	256	16384

Table 12: MPPT timing configuration with SRCx_CFG[4:3] pins



6.3. Source Constant Voltage Regulation

The following configurations apply when **SRCx_MODE** is LOW, so that the boost converter is in constant voltage mode. The user can set the regulation voltage with **SRCx_CFG[4:0]** (see Table 13), or through the **SRCxREGUx** registers (see Section 9.3).

Configuration pins					Voltage [V]
SRCx_CFG[4:0]					$V_{SRCx,REG}$
L	L	L	L	L	0.143
L	L	L	L	H	0.300
L	L	L	H	L	0.360
L	L	L	H	H	0.420
L	L	H	L	L	0.480
L	L	H	L	H	0.510
L	L	H	H	L	0.525
L	L	H	H	H	0.540
L	H	L	L	L	0.555
L	H	L	L	H	0.570
L	H	L	H	L	0.600
L	H	L	H	H	0.660
L	H	H	L	L	0.720
L	H	H	L	H	0.735
L	H	H	H	L	0.750
L	H	H	H	H	0.765
Configuration pins					Voltage [V]
SRCx_CFG[4:0]					$V_{SRCx,REG}$
H	L	L	L	L	0.780
H	L	L	L	H	0.810
H	L	L	H	L	0.870
H	L	L	H	H	0.930
H	L	H	L	L	0.990
H	L	H	L	H	1.095
H	L	H	H	L	1.200
H	L	H	H	H	1.305
H	H	L	L	L	1.395
H	H	L	L	H	1.500
H	H	L	H	L	1.612
H	H	L	H	H	1.701
H	H	H	L	L	1.791
H	H	H	L	H	1.903
H	H	H	H	L	1.993
H	H	H	H	H	2.104

Table 13: Configuration of the source constant voltage regulation with **SRCx_CFG[4:0]** pins



6.4. Storage Element Thresholds

The storage element protection thresholds V_{OVCH} , V_{CHRDY} and V_{OVCH} , can be configured through the **STO_CFG[2:0]** pins as shown in Table 14.

Configuration pins			Overdischarge voltage [V]	Charge ready voltage [V]	Overcharge voltage [V]	Battery Type
STO_CFG[2:0]			V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
L	L	L	2.50	2.55	3.80	Lithium-ion Super Capacitor (LiC)
L	L	H	2.50	2.55	3.50	Lithium-ion Super Capacitor 85 °C (LiC)
L	H	L	3.00	3.30	4.12	Lithium-ion
L	H	H	3.00	3.30	3.90	Lithium-ion (long life)
H	L	L	3.50	3.55	3.90	Lithium-ion (super long life)
H	L	H	3.00	3.30	4.12	Lithium Polymer (LiPo)
H	H	L	2.80	3.10	3.63	Lithium Iron Phosphate (LiFePO4)
H	H	H	2.60	2.80	3.80	Tadiran HLC1020

Table 14: Storage element configuration with **STO_CFG[2:0]** pins

DISCLAIMER: storage element thresholds provided in the table above are indicative to support a wide range of storage element variants. They are provided as is to the best knowledge of e-peas's application laboratory. They should not replace the actual values provided in the storage element manufacturer's specifications and datasheet.



6.5. Boost Converter Timings

The boost converter timing multiplier default value is:

- x3, when I²C configuration is not used.
- x2, when I²C configuration is used.

Please refer to Table 34 for the different L_{BOOSTx} values for each timing multiplier value.

To configure a different boost timing multiplier value, and thus, configure the peak current of the boost converter inductor, see Section 9.5 (available by I²C register only).

6.6. Buck Converter

6.6.1. Load Voltage

Table 15 shows how to configure the regulated voltage on **LOAD** output with the **LOAD_CFG[2:0]** pins.

Configuration pins			LOAD voltage [V]
LOAD_CFG[2:0]			V_{LOAD}
L	L	L	Buck disabled
L	L	H	0.6
L	H	L	0.9
L	H	H	1.2
H	L	L	1.5
H	L	H	1.8
H	H	L	2.2
H	H	H	2.5 ¹

Table 15: Configuration of LOAD voltage with LOAD_CFG[2:0] pins

1. This configuration is only available if $V_{OVDIS} \geq 2.5$ V.

6.6.2. Buck Converter Timings

The buck converter timing multiplier default value is:

- x2, when I²C configuration is not used.
- x4, when I²C configuration is used.

Please refer to Table 36 for the different L_{BUCK} values for each timing multiplier value.

To configure a different buck timing multiplier value, and thus, configure the peak current of the buck converter inductor, see Section 9.6 (available by I²C register only).

6.7. Thermal Monitoring

Thermal monitoring is configured by applying the following equations to determine a temperature threshold value to be written in registers TEMP_COLDCH, TEMP_HOTCH, TEMP_COLDDIS or TEMP_HOTDIS:

$$\begin{aligned} THRES &= \frac{256 \cdot R_{TH}(T)}{R_{TH}(T) + R_{DIV}} \\ R_{TH}(T) &= R_0 \cdot e^{B \cdot \left(\frac{1}{T} - \frac{1}{T_0} \right)} \\ T &= \frac{B}{\ln\left(\frac{R_{TH}(T)}{R_0}\right) + \frac{B}{T_0}} \end{aligned}$$

- THRES is the unsigned 8-bit value to be written in the registers to set the temperature threshold to the temperature T [K].
- R₀ [Ω] is the resistance of the NTC thermistor at ambient temperature T₀ = 298.15 K (25 °C).
- R_{TH}(T) [Ω] is the resistance of the thermistor at temperature T [K].
- T₀ [K] = 298.15 K (25 °C)
- T [K] is the current ambient temperature of the circuit.
- B is the characteristic constant of the thermistor, allowing to determine the resistance of the thermistor for a given temperature.

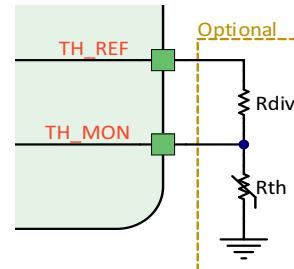


Figure 10: TH_REF and TH_MON connections

The typical values of R_{TH} and R_{DIV}, found in Table 9, allow for having a range of -25 °C to +70 °C for both charging and discharging.

Please note that the thermistor must be of the NTC (Negative Temperature Coefficient) type.



6.8. 5 V Charger

The 5 V charger implements CC/CV operation. When in CC, the maximum charging current $I_{5V,CC}$ can be set by connecting a resistor $R_{5V,IMAX}$ between $5V_IMAX$ and GND:

$$I_{5V,CC} = \frac{50}{R_{5V,MAX}}$$

Please note that, $R_{5V,IMAX}$ must be chosen so that $I_{5V,CC}$ complies with the range defined in Table 7. Example values can be found in Table 16:

Resistor [Ω]	Maximum Charging Current [mA]
$R_{5V,IMAX}$	$I_{5V,CC}$
370	135.0
680	73.5
1500	33.3
3700	13.5

Table 16: Typical resistor values for setting 5 V charger max. current

Please note that, the rise time of the voltage applied on the $5V_IN$ pin must not be too short. Thus, it is recommended to add a RC circuit in series with the $5V_IN$ pin which matches the following, with R_{5V} in series and C_{5V} between $5V_IN$ and GND:

$$R_{5V} \cdot C_{5V} > T_{5V,RISE}$$

- $T_{5V,RISE}$ is the minimum rise time from 0 V to 5 V of the voltage on the $5V_IN$ pin (see Table 7). Comparing this to the RC constant adds a margin as the RC constant defines 63% of the final voltage.
- R_{5V} must be determined so that, for the configured $I_{5V,CC}$, the voltage on the $5V_IN$ pin is:
 - above 3.5 V.
 - above $V_{STO} + 200$ mV.
- C_{5V} is determined from the value of R_{5V} using the equation above. A low charging current allows for high R_{5V} value and thus, for a low C_{5V} value.

6.9. Shipping Mode

The shipping mode, described in Section 5.8, is enabled by connecting the $SHIP_MODE$ pin to $VINT$ and disabled by connecting the $SHIP_MODE$ pin to GND or by leaving it floating.



7. I²C Serial Interface Protocol

The AEM13920 uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (**SDA**) and a serial clock line (**SCL**). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

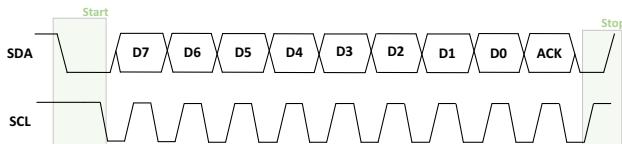


Figure 11: I²C transmission frame

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The AEM13920 is a slave that will receive configuration data or send the informations requested by the master.

The AEM13920 supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data are sent with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled-up (**SDA** and **SCL** are open drain outputs);
- Start bit (S): to initiates the transmission, the master switches the **SDA** line low while keeping **SCL** high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the **SDA** line from low to high while keeping **SCL** high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches **SDA** low;
- NACK: when the device receiving data keeps **SDA** high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x41 for the AEM13920.

- Bit [0] is the communication mode: 1 for 'read mode' (used when the master reads informations from the slave) and 0 for 'write mode' (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

Here is the procedure for the master to write a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the TEMPCHOLDC register, the master sends the value 0x0B;
- Slave sends an ACK;
- Master sends the data to write to the register;
- Slave sends an ACK;
- If the master wants to write register at the next address (TEMPHOTCH in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several consecutive registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the APM0BUCK register, the master sends the value 0x1F;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in 'read' mode;
- Slave sends an ACK;
- Master provides the clock on **SCL** to allow the slave to shift the data of the read register on **SDA**;
- If the master wants to read register at the next address (APM1BUCK in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for writing several registers;
- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in Figure 12. Refer to Table 17 for all register addresses.

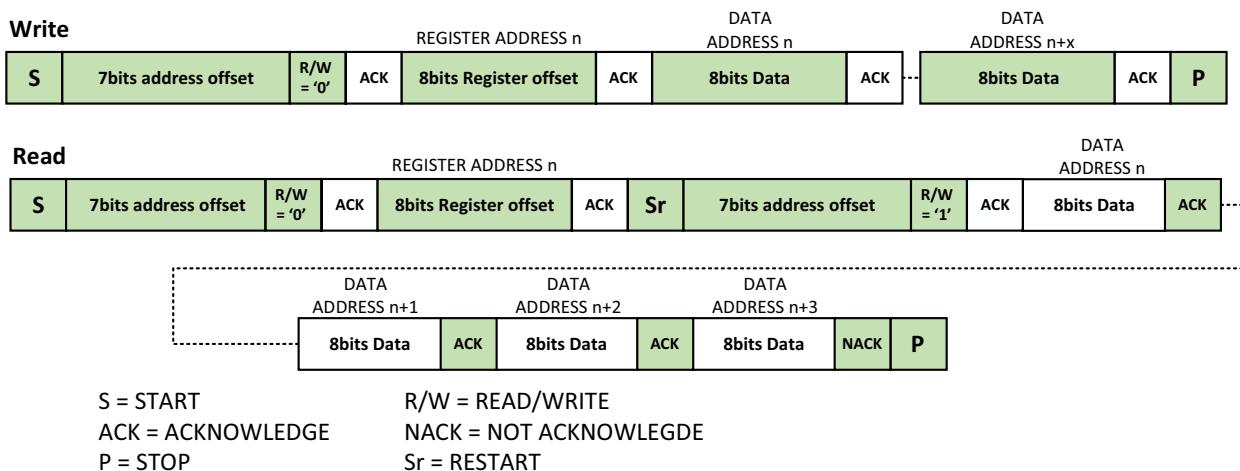


Figure 12: Read and write transmission



8. Register Map

Please note that the AEM13920 device address is 0x41.

Address	Name	Bit	Field Name	Access	Reset	Description
0x00	VERSION	[3:0]	MINOR	R	-	Minor version number.
		[7:4]	MAJOR	R	-	Major version number.
0x01	SRC1REGU0	[0:0]	MODE	R/W	0x01	SRC1 regulation mode.
		[3:1]	CFG0	R/W	0x00	SRC1 regulation mechanism configuration.
0x02	SRC1REGU1	[2:0]	CFG1	R/W	0x00	
		[5:3]	CFG2	R/W	0x00	
0x03	SRC2REGU0	[0:0]	MODE	R/W	0x01	SRC2 regulation mode.
		[3:1]	CFG0	R/W	0x00	SRC2 regulation mechanism configuration.
0x04	SRC2REGU1	[2:0]	CFG1	R/W	0x00	
		[5:3]	CFG2	R/W	0x00	
0x05	VOVDIS	[5:0]	THRESH	R/W	0x06	Storage element overdischarge threshold.
0x06	VCHRDY	[5:0]	THRESH	R/W	0x05	Storage element ready threshold.
0x07	VOVCH	[6:0]	THRESH	R/W	0x3A	Storage element overcharge threshold.
0x08	BST1CFG	[0:0]	EN	R/W	0x01	Boost SRC1 enable.
		[1:1]	HPEN	R/W	0x01	Boost SRC1 high-power mode enable.
		[4:2]	TMULT	R/W	0x01	Boost SRC1 current configuration.
0x09	BST2CFG	[0:0]	EN	R/W	0x01	Boost SRC2 enable.
		[1:1]	HPEN	R/W	0x01	Boost SRC2 high-power mode enable.
		[4:2]	TMULT	R/W	0x01	Boost SRC2 current configuration.
0x0A	BUCKCFG	[2:0]	VOUT	R/W	0x00	Buck voltage configuration.
		[5:3]	TMULT	R/W	0x03	Buck current configuration.
0x0B	TEMPCOLDCH	[7:0]	THRESH	R/W	0xD1	Cold temperature threshold for storage element charging.
0x0C	TEMPHOTCH	[7:0]	THRESH	R/W	0x18	Hot temperature threshold for storage element charging.
0x0D	TEMPCOLDDIS	[7:0]	THRESH	R/W	0xD1	Cold temperature threshold for storage element discharging.
0x0E	TEMPHOTDIS	[7:0]	THRESH	R/W	0x18	Hot temperature threshold for storage element discharging.
0x0F	TMON	[0:0]	EN	R/W	0x01	Temperature monitoring enable.
0x10	SRCLOW	[2:0]	SRC1THRESH	R/W	0x00	V_{SRCLOW} threshold for SRC1 .
		[5:3]	SRC2THRESH	R/W	0x00	V_{SRCLOW} threshold for SRC2 .
0x11	APM	[0:0]	SRC1EN	R/W	0x00	APM SRC1 enable.
		[1:1]	SRC2EN	R/W	0x00	APM SRC2 enable.
		[2:2]	BUCKEN	R/W	0x00	APM LOAD enable.
		[3:3]	RSVD1	R/W	0x00	APM reserved 1.
		[4:4]	RSVD2	R/W	0x00	APM reserved 2.

Table 17: Register map (part 1)



Address	Name	Bit	Field Name	Access	Reset	Description
0x12	IRQENO	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable.
		[1:1]	VOVDIS	R/W	0x00	IRQ VOVDIS enable.
		[2:2]	VCHRDY	R/W	0x00	IRQ VCHRDY enable.
		[3:3]	VOVCH	R/W	0x00	IRQ VOVCH enable.
		[4:4]	SRCLOW	R/W	0x00	IRQ source low threshold (SRCx) enable.
		[5:5]	TEMPCH	R/W	0x00	IRQ temperature (charge) enable.
		[6:6]	TEMPDIS	R/W	0x00	IRQ temperature (discharge) enable.
0x13	IRQEN1	[0:0]	SRC1MPPTSTART	R/W	0x00	IRQ MPPT start (SRC1) enable.
		[1:1]	SRC1MPPTDONE	R/W	0x00	IRQ MPPT done (SRC1) enable.
		[2:2]	SRC2MPPTSTART	R/W	0x00	IRQ MPPT start (SRC2) enable.
		[3:3]	SRC2MPPTDONE	R/W	0x00	IRQ MPPT done (SRC2) enable.
		[4:4]	STODONE	R/W	0x00	IRQ STO ADC done enable.
		[5:5]	TEMPDONE	R/W	0x00	IRQ temperature ADC done enable.
		[6:6]	APMDONE	R/W	0x00	IRQ APM done enable.
		[7:7]	APMERR	R/W	0x00	IRQ APM error enable.
0x14	CTRL	[0:0]	UPDATE	R/W	0x00	Load I ² C registers configuration.
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag.
0x15	IRQFLG0	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag.
		[1:1]	VOVDIS	R	0x00	IRQ VOVDIS flag.
		[2:2]	VCHRDY	R	0x00	IRQ VCHRDY flag.
		[3:3]	VOVCH	R	0x00	IRQ VOVCH flag.
		[4:4]	SRCLOW	R	0x00	IRQ source low threshold (SRCx) flag.
		[5:5]	TEMPCH	R	0x00	IRQ temperature (charge) flag.
		[6:6]	TEMPDIS	R	0x00	IRQ temperature (discharge) flag.
0x16	IRQFLG1	[0:0]	SRC1MPPTSTART	R	0x00	IRQ MPPT start (SRC1) flag.
		[1:1]	SRC1MPPTDONE	R	0x00	IRQ MPPT done (SRC1) flag.
		[2:2]	SRC2MPPTSTART	R	0x00	IRQ MPPT start (SRC2) flag.
		[3:3]	SRC2MPPTDONE	R	0x00	IRQ MPPT done (SRC2) flag.
		[4:4]	STODONE	R	0x00	IRQ STO ADC done flag.
		[5:5]	TEMPDONE	R	0x00	IRQ temperature ADC done flag.
		[6:6]	APMDONE	R	0x00	IRQ APM done flag.
		[7:7]	APMERR	R	0x00	IRQ APM error flag.
0x17	STATUS0	[0:0]	VOVDIS	R	0x00	Status VOVIDS.
		[1:1]	VCHRDY	R	0x00	Status VCHRDY.
		[2:2]	VOVCH	R	0x00	Status VOVCH.
		[3:3]	SRC1SRCLOW	R	0x00	Status source low threshold (SRC1).
		[4:4]	SRC2SRCLOW	R	0x00	Status source low threshold (SRC2).
0x18	STATUS1	[0:0]	TEMPCOLDCH	R	0x00	Status cold temperature (charge).
		[1:1]	TEMPHOTCH	R	0x00	Status hot temperature (charge).
		[2:2]	TEMPCOLDDIS	R	0x00	Status cold temperature (discharge).
		[3:3]	TEMPHOTDIS	R	0x00	Status hot temperature (discharge).
0x19	APM0SRC1	[7:0]	DATA	R	0x00	APM data 0 (SRC1).
0x1A	APM1SRC1	[7:0]	DATA	R	0x00	APM data 1 (SRC1).
0x1B	APM2SRC1	[7:0]	DATA	R	0x00	APM data 2 (SRC1).

Table 17: Register map (part 2)



Address	Name	Bit	Field Name	Access	Reset	Description
0x1C	APM0SRC2	[7:0]	DATA	R	0x00	APM data 0 (SRC2).
0x1D	APM1SRC2	[7:0]	DATA	R	0x00	APM data 1 (SRC2).
0x1E	APM2SRC2	[7:0]	DATA	R	0x00	APM data 2 (SRC2).
0x1F	APM0BUCK	[7:0]	DATA	R	0x00	APM data 0 (BUCK).
0x20	APM1BUCK	[7:0]	DATA	R	0x00	APM data 1 (BUCK).
0x21	APM2BUCK	[7:0]	DATA	R	0x00	APM data 2 (BUCK).
0x22	APMERR	[0:0]	SRC1ERR	R	0x00	APM SRC1 error.
		[1:1]	SRC1NVLD	R	0x00	APM corrupted SRC1 .
		[2:2]	SRC2ERR	R	0x00	APM SRC2 error.
		[3:3]	SRC2NVLD	R	0x00	APM corrupted SRC2 .
		[4:4]	BUCKERR	R	0x00	APM BUCK error.
		[5:5]	BUCKNVLD	R	0x00	APM corrupted BUCK.
0x23	TEMP	[7:0]	DATA	R	0x00	Temperature monitoring value.
0x24	STO	[7:0]	DATA	R	0x00	Storage monitoring value.
0x25	SRC1	[7:0]	DATA	R	0x00	SRC1 monitoring value.
0x26	SRC2	[7:0]	DATA	R	0x00	SRC2 monitoring value.

Table 17: Register map (part 3)



9. Registers Configuration

9.1. I²C Control (CTRL)

Control register.

CTRL Register	0x14			R/W
Bit [7:3]	Bit [2]	Bit [1]	Bit [0]	
RESERVED	SYNCBUSY	RESERVED	UPDATE	
0x00	0	0	0	

Table 18: CTRL register

Bit [2]: SYNCBUSY (CTRL.SYNCBUSY).

This field indicates whether the synchronization from the I²C registers to the system registers is ongoing or not.

- 0: NSYNC - R: CTRL register not synchronizing.
- 1: SYNC - R: CTRL register synchronizing.

Bit [0]: UPDATE (CTRL.UPDATE).

This field is used to control the source of the AEM13920 configuration (GPIO or I²C).

Furthermore, this field is used to update the AEM13920 configuration with the current configuration from the I²C registers.

- 0: GPIO
 - W: load configurations from the GPIO.
 - R: configurations from the GPIO is currently used if read as 0.
- 1: I²C
 - W: load configurations from the I²C registers.
 - R: configurations from the I²C is currently used if read as 1.

NOTE: if the AEM13920 is already configured through the I²C registers, writing any register does not have any effect until 1 is written to the CTRL.UPDATE field, leading to the AEM13920 to read the new register values and apply them.

NOTE: when using I²C register configuration, user can switch back to GPIO configuration by writing 0 to the CTRL.UPDATE field. In that case, the settings previously written to the IRQEN registers are still valid even when using GPIO configuration, as well as the data in IRQFLG register.

9.2. Version Register (VERSION)

The VERSION register holds the version of the chip, with major and minor revision numbers.

VERSION Register	0x00		R
Bit [7:4]	Bit [3:0]		
MAJOR	MINOR		
-	-	-	

Table 19: VERSION register

Bit [7:4]: major version number (VERSION.MAJOR).

Bit [3:0]: minor version number (VERSION.MINOR).



9.3. Source Regulation Configuration Registers (SRCxREGUx)

The SRCxREGUx registers allow for configuring SRCx regulation.

Table 20 shows the use of SRCxREGUx registers according to the source regulation mode.

- **SRCxREGU0.MODE = 0:** constant voltage regulation mode, as described in Section 9.3.3 and Table 23.
- LVL [7:0] - Defines the constant regulation voltage.

- **SRCxREGU0.MODE = 1:** MPPT regulation mode, as described in Section 9.3.4 and in Tables 24, 25 and 26.
 - MPPT_RATIO [2:0] - defines the MPPT ratio.
 - MPPT_SAMPLING [2:0] - defines the MPPT sampling time.
 - MPPT_PERIOD [2:0] - defines the MPPT period.

Register Field	SRCxREGU1								SRCxREGU0							
	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Mode 0 Constant Voltage			CFG2			CFG1								CFG0		MODE
Mode 1 MPPT			LVL[7:6]	LVL[5:3]	MPPT_PERIOD [2:0]	MPPT_SAMPLING [2:0]							MPPT_RATIO [2:0]	LVL [2:0]	MODE	

Table 20: Summary of SRCxREGUx register fields

9.3.1. SRCxREGU0

SRCxREGU0 are the first configuration registers for configuring SRCx regulation voltage mechanism.

Please note that, when SRCxREGU0 = 0, SRCxREGU1.CFG2 [2] (SRCxREGU1 [5]) is not used.

SRC1REGU0 Register	0x01	R/W
SRC2REGU0 Register	0x03	R/W
Bit [7:4]	Bit [3:1]	Bit [0]
RESERVED	CFG0	MODE
0x00	0x00	1

Table 21: SRCxREGU0 register

Bit [3:1]: SRCx configuration 0 (SRCxREGU0.CFG0).

This fields is used to configure SRCx regulation mechanism. Depending on MODE value, this fields is used to configure the following parameters:

- **MODE = 0:** SRCx regulation voltage, along with the other SRCxREGUx.CFGx registers fields.
- **MODE = 1:** ratio/ZMPP, as set by other SRCxREGUx.CFGx registers fields.

Bit [0]: SRCx regulation mode (SRCxREGU0.MODE).

This fields is used to configure SRCx regulation mode:

- 0: select regulation as constant voltage.
- 1: select regulation as MPPT (V_{MPP} / V_{OC} or ZMPP).



9.3.2. SRCxREGU1

SRCxREGU1 are the second configuration registers for configuring SRCx regulation voltage mechanism.

SRC1REGU1 Register		0x02	R/W
SRC2REGU1 Register		0x04	R/W
Bit [7:6]	Bit [5:3]	Bit [2:0]	
RESERVED	CFG2	CFG1	
0x00	0x00	0x00	

Table 22: SRCxREGU1 register

Bit [5:3]: SRCx configuration 2 (SRCxREGU1.CFG2).

This fields is used to configure SRCx regulation mechanism. Depending on MODE value, this fields is used to configure the following parameters:

- MODE = 0: SRCx regulation voltage, along with the other SRCxREGUx.CFGx registers fields.
- MODE = 1: SRCx MPPT sampling duration $T_{MPPT,SAMPLING}$.

Bit [2:0]: SRCx configuration 1 (SRCxREGU1.CFG1).

This fields is used to configure SRCx regulation mechanism. Depending on MODE value, this fields is used to configure the following parameters:

- MODE = 0: regulation voltage, along with the other SRCxREGUx.CFGx registers fields.
- MODE = 1: SRCx MPPT period $T_{MPPT,PERIOD}$.



9.3.3. Constant Voltage Configuration

Table 23 describes how to configure SRCxREGUx registers when the AEM13920 source regulation mode is set to constant voltage.

See Table 20 for a description of how LVL [7:0] is distributed across SRCxREGUx registers.

LVL [7:0]	V _{SRCx,REG} [V]								
0x00		0x2A	0.375	0x4A	0.855	0x6A	1.335	0x8A	1.970
...	Source Low ¹	0x2B	0.390	0x4B	0.870	0x6B	1.350	0x8B	1.993
0x0C		0x2C	0.405	0x4C	0.885	0x6C	1.365	0x8C	2.015
0x0D	0.120	0x2D	0.420	0x4D	0.900	0x6D	1.380	0x8D	2.037
0x0E	0.128	0x2E	0.435	0x4E	0.915	0x6E	1.395	0x8E	2.060
0x0F	0.135	0x2F	0.450	0x4F	0.930	0x6F	1.410	0x8F	2.082
0x10	0.143	0x30	0.465	0x50	0.945	0x70	1.425	0x90	2.104
0x11	0.150	0x31	0.480	0x51	0.960	0x71	1.440	0x91	2.127
0x12	0.158	0x32	0.495	0x52	0.975	0x72	1.455	0x92	2.149
0x13	0.165	0x33	0.510	0x53	0.990	0x73	1.470	0x93	2.172
0x14	0.173	0x34	0.525	0x54	1.005	0x74	1.478	0x94	2.194
0x15	0.180	0x35	0.540	0x55	1.020	0x75	1.500	0x95	2.227
0x16	0.188	0x36	0.555	0x56	1.035	0x76	1.522	0x96	2.273
0x17	0.195	0x37	0.570	0x57	1.050	0x77	1.545	0x97	2.318
0x18	0.203	0x38	0.585	0x58	1.065	0x78	1.567	0x98	2.364
0x19	0.210	0x39	0.600	0x59	1.080	0x79	1.590	0x99	2.409
0x1A	0.218	0x3A	0.615	0x5A	1.095	0x7A	1.612	0x9A	2.455
0x1B	0.225	0x3B	0.630	0x5B	1.110	0x7B	1.634	0x9B	2.500
0x1C	0.233	0x3C	0.645	0x5C	1.125	0x7C	1.657	0x9C	2.545
0x1D	0.240	0x3D	0.660	0x5D	1.140	0x7D	1.679	0x9D	2.591
0x1E	0.248	0x3E	0.675	0x5E	1.155	0x7E	1.701	0x9E	2.636
0x1F	0.255	0x3F	0.690	0x5F	1.170	0x7F	1.724	0x9F	2.682
0x20	0.263	0x40	0.705	0x60	1.185	0x80	1.746	0xA0	2.727
0x21	0.270	0x41	0.720	0x61	1.200	0x81	1.769	0xA1	2.773
0x22	0.278	0x42	0.735	0x62	1.215	0x82	1.791	0xA2	2.818
0x23	0.285	0x43	0.750	0x63	1.230	0x83	1.813	0xA3	2.864
0x24	0.293	0x44	0.765	0x64	1.245	0x84	1.836	0xA4	2.909
0x25	0.300	0x45	0.780	0x65	1.260	0x85	1.858	0xA5	2.955
0x26	0.315	0x46	0.795	0x66	1.275	0x86	1.881	0xA6	3.000
0x27	0.330	0x47	0.810	0x67	1.290	0x87	1.903	0xA7	3.045
0x28	0.345	0x48	0.825	0x68	1.305	0x88	1.925	0xA8	3.091
0x29	0.360	0x49	0.840	0x69	1.320	0x89	1.948	0xA9	3.136
							0xFF
									4.455

Table 23: SRCx constant voltage values configured by SRCxREGUx (SRCxREGU0.MODE = 0)

1. Setting SRCxREGUx.LVL to a value less than 0x0D causes the AEM13920 to consider the SRCx voltage to be less than V_{SRCLOW}, which may cause the AEM13920 to enter SLEEP STATE if the SLEEP condition is met.



9.3.4. MPPT Configuration

This section describes how to configure the MPPT module through the SRCxREGUx registers.

See Table 20 for the distribution of MPPT_RATIO [2:0], MPPT_SAMPLING [2:0], MPPT_PERIOD [2:0] values across SRCxREGUx registers.

- Table 24 shows the configuration of SRCxREGU0.CFG0 register field to set the MPPT ratio.
- Table 25 shows the configuration of SRCxREGU1.CFG1 register field to set the MPPT sampling duration.
- Table 26 shows the configuration of SRCxREGU1.CFG2 register field to set the MPPT period.

SRCxREGU0.CFG0 MPPT_RATIO [2:0]			R _{MPPT} / ZMPP
0	0	0	35 %
0	0	1	50 %
0	1	0	65 %
0	1	1	70 %
1	0	0	75 %
1	0	1	80 %
1	1	0	85 %
1	1	1	SRC1: ZMPP SRC2: 100 %

Table 24: SRCx MPPT ratio/ZMPP configured by SRCxREGUx
(SRCxREGU0.MODE = 1)

SRCxREGU1.CFG1 MPPT_SAMPLING [2:0]			T _{MPPT,SAMPLING} [ms]
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	128
1	1	0	256
1	1	1	512

Table 25: SRCx MPPT sampling duration configured by SRCxREGUx (SRCxREGU0.MODE = 1)

SRCxREGU1.CFG2 MPPT_PERIOD [2:0]			T _{MPPT,PERIOD} [ms]
0	0	0	128
0	0	1	256
0	1	0	512
0	1	1	1024
1	0	0	2048
1	0	1	4096
1	1	0	8192
1	1	1	16384

Table 26: SRCx MPPT period configured by SRCxREGUx
(SRCxREGU0.MODE = 1)



9.4. Storage Element Threshold Voltages (VOVDIS / VCHRDY / VOVCH)

The storage element protection thresholds, described in Section 6.4, can be set independently by the registers VOVDIS, VCHRDY and VOVCH.

9.4.1. Overdischarge Voltage (VOVDIS)

The VOVDIS register allows for configuring V_{OVDIS} , as shown in Table 28.

VOVDIS Register		0x05	R/W
Bit [7:6]	Bit [5:0]		
RESERVED		THRESH	
0x00	0x06		

Table 27: VOVDIS register

VOVDIS [5:0]	V_{OVDIS} [V]						
0x00	2.400	0x10	2.700	0x20	3.000	0x30	3.300
0x01	2.419	0x11	2.719	0x21	3.019	0x31	3.319
0x02	2.438	0x12	2.738	0x22	3.038	0x32	3.338
0x03	2.456	0x13	2.756	0x23	3.056	0x33	3.356
0x04	2.475	0x14	2.775	0x24	3.075	0x34	3.375
0x05	2.494	0x15	2.794	0x25	3.094	0x35	3.394
0x06	2.513	0x16	2.813	0x26	3.113	0x36	3.413
0x07	2.531	0x17	2.831	0x27	3.131	0x37	3.431
0x08	2.550	0x18	2.850	0x28	3.150	0x38	3.450
0x09	2.569	0x19	2.869	0x29	3.169	0x39	3.469
0x0A	2.588	0x1A	2.888	0x2A	3.188	0x3A	3.488
0x0B	2.606	0x1B	2.906	0x2B	3.206	0x3B	3.506
0x0C	2.625	0x1C	2.925	0x2C	3.225	0x3C	3.525
0x0D	2.644	0x1D	2.944	0x2D	3.244	0x3D	3.544
0x0E	2.663	0x1E	2.963	0x2E	3.263	0x3E	3.563
0x0F	2.681	0x1F	2.981	0x2F	3.281	0x3F	3.581

Table 28: Storage element V_{OVDIS} configuration by VOVDIS register



9.4.2. Charge Ready Voltage (VCHRDY)

The VCHRDY register allows for configuring V_{CHRDY} , as shown in Table 30.

VCHRDY Register		0x06	R/W
Bit [7:6]	Bit [5:0]		
RESERVED		THRESH	
0x00	0x05		

Table 29: VCHRDY register

VCHRDY [5:0]	V _{CHRDY} [V]						
0x00	2.456	0x10	2.756	0x20	3.056	0x30	3.356
0x01	2.475	0x11	2.775	0x21	3.075	0x31	3.375
0x02	2.494	0x12	2.794	0x22	3.094	0x32	3.394
0x03	2.512	0x13	2.812	0x23	3.112	0x33	3.412
0x04	2.531	0x14	2.831	0x24	3.131	0x34	3.431
0x05	2.550	0x15	2.850	0x25	3.150	0x35	3.450
0x06	2.569	0x16	2.869	0x26	3.169	0x36	3.469
0x07	2.587	0x17	2.887	0x27	3.187	0x37	3.487
0x08	2.606	0x18	2.906	0x28	3.206	0x38	3.506
0x09	2.625	0x19	2.925	0x29	3.225	0x39	3.525
0x0A	2.644	0x1A	2.944	0x2A	3.244	0x3A	3.544
0x0B	2.662	0x1B	2.962	0x2B	3.262	0x3B	3.562
0x0C	2.681	0x1C	2.981	0x2C	3.281	0x3C	3.581
0x0D	2.700	0x1D	3.000	0x2D	3.300	0x3D	3.600
0x0E	2.719	0x1E	3.019	0x2E	3.319	0x3E	3.619
0x0F	2.737	0x1F	3.037	0x2F	3.337	0x3F	3.637

Table 30: Storage element V_{CHRDY} configuration by VCHRDY register



9.4.3. Overcharge Voltage (VOVCH)

The VOVCH register allows for the configuration of V_{OVCH} , as shown in Table 32.

VOVCH Register		0x07	R/W
Bit [7]		Bit [6:0]	
RESERVED		THRESH	
0x00		0x3A	

Table 31: VOVCH register

VOVCH	V_{OVCH} [V]						
0x00	2.700	0x1B	3.206	0x36	3.713	0x51	4.219
0x01	2.719	0x1C	3.225	0x37	3.731	0x52	4.238
0x02	2.738	0x1D	3.244	0x38	3.750	0x53	4.256
0x03	2.756	0x1E	3.263	0x39	3.769	0x54	4.275
0x04	2.775	0x1F	3.281	0x3A	3.788	0x55	4.294
0x05	2.794	0x20	3.300	0x3B	3.806	0x56	4.313
0x06	2.813	0x21	3.319	0x3C	3.825	0x57	4.331
0x07	2.831	0x22	3.338	0x3D	3.844	0x58	4.350
0x08	2.850	0x23	3.356	0x3E	3.863	0x59	4.369
0x09	2.869	0x24	3.375	0x3F	3.881	0x5A	4.388
0x0A	2.888	0x25	3.394	0x40	3.900	0x5B	4.406
0x0B	2.906	0x26	3.413	0x41	3.919	0x5C	4.425
0x0C	2.925	0x27	3.431	0x42	3.938	0x5D	4.444
0x0D	2.944	0x28	3.450	0x43	3.956	0x5E	4.463
0x0E	2.963	0x29	3.469	0x44	3.975	0x5F	4.481
0x0F	2.981	0x2A	3.488	0x45	3.994	0x60	4.500
0x10	3.000	0x2B	3.506	0x46	4.013	0x61	4.519
0x11	3.019	0x2C	3.525	0x47	4.031	0x62	4.538
0x12	3.038	0x2D	3.544	0x48	4.050	0x63	4.556
0x13	3.056	0x2E	3.563	0x49	4.069	0x64	4.575
0x14	3.075	0x2F	3.581	0x4A	4.088	0x65	4.594
0x15	3.094	0x30	3.600	0x4B	4.106		
0x16	3.113	0x31	3.619	0x4C	4.125		
0x17	3.131	0x32	3.638	0x4D	4.144		
0x18	3.150	0x33	3.656	0x4E	4.163		
0x19	3.169	0x34	3.675	0x4F	4.181		
0x1A	3.188	0x35	3.694	0x50	4.200		
					
						0x7F	4.594

Table 32: Storage element V_{OVCH} configuration by VOVCH register



9.5. Boost Converters (BSTxCFG)

The settings of the boost converters can be configured with registers BSTxCFG.

BST1CFG Register	0x08	R/W	
BST2CFG Register	0x09	R/W	
Bit [7:5]	Bit [4:2]	Bit [1]	Bit [0]
RESERVED	TMULT	HPEN	EN
0x00	0x01 ¹	1	1

Table 33: BSTxCFG registers

1. The boost converter timing multiplier default value is different depending on whether the AEM13920 is configured by I²C or not. See Section 6.5 for the default values of each configuration method.

Bit [4:2]: boost converter timing configuration (TMULT)

This field allows for modifying the peak current of the boost inductor by increasing/decreasing the on/off timings of the boost converter. The higher the timing multiplier, the higher the boost inductor peak current, and thus the higher the average source current pulled from SRCx to STO.

The peak current in the inductor also depends on the value of the inductor.

Bit [1]: boost converter high power mode enable (ENHP)

Setting this bit to 1 allows the AEM13920 to automatically enter high-power mode if needed, allowing for more power to be harvested from SRCx (see Section 5.2.4).

Setting this bit to 0 disables automatic high-power mode.

Bit [0]: enable boost converter (EN)

Setting this bit to 1 enables the corresponding boost converter. Setting it to 0 disables it.

TMULT	Timing Multiplier	Minimum L _{BOOSTx} [μ H] ¹	L _{BOOSTx} for best efficiency [μ H] ²
0x00	x1	3.3	15
0x01	x2	6.6	33
0x02	x3	9.9	47
0x03	x4	13.2	68
0x04	x6	19.8	100
0x05	x8	26.4	120
0x06	x12	39.6	180
0x07	x16	52.8	220

Table 34: Boost inductor values according to boost timing

1. Never install an inductor with an inductance (real value including tolerance, derating, etc.) lower than those values for each setting of the timing multiplier. This would cause permanent damage to the AEM13920.
2. Those values provide the best efficiency according to the tests carried out in the e-peas laboratory.



9.6. Buck Converter (BUCKCFG)

This register allows for configuring the buck converter, which output is the **LOAD** pin.

BUCKCFG Register		0x0A	R/W
Bit [7:6]	Bit [5:3]	Bit [2:0]	
RESERVED	TMULT	VOUT	
0x00	0x03 ¹	0x00	

Table 35: BUCKCFG register

1. The buck converter timing multiplier default value is different depending on whether the AEM13920 is configured by I²C or not. See Section 6.6.2 for the default values of each configuration method.

Bit [5:3]: buck converter timing configuration (TMULT)

This field allows for modifying the peak current of the buck inductor by increasing/decreasing the on/off timings of the buck converter. The higher the timing multiplier, the higher the buck inductor peak current, and thus the higher the average current pulled from **STO** to **LOAD**.

The peak current in the inductor depends also on the value of the inductor. Table 36 shows the minimum inductor value that can be used for each timing without damaging the AEM13920.

TMULT	Timing Multiplier	Minimum L _{BUCK} [μH] ¹	L _{BUCK} for best efficiency [μH] ²
0x00	x1	1.7	3.3
0x01	x2	3.3	6.8
0x02	x3	5.0	10
0x03	x4	6.6	15
0x04	x6	9.9	22
0x05	x8	13.2	33
0x06	x12	19.8	47
0x07	x16	26.4	68

Table 36: Buck inductor values according to buck timing

- Never install an inductor with an inductance (real value including tolerance, derating, etc.) lower than those values for each setting of the timing multiplier. This would cause permanent damage to the AEM13920.
- Those values provide the best efficiency according to the tests carried out in the e-peas laboratory.

Bit [2:0]: buck converter output regulation voltage (VOUT)

This field allows for setting the regulation output voltage V_{LOAD} of the buck converter (supplying the **LOAD** pin). The available voltages can be found in Table 37. To switch off the buck converter, set BUCK.VOUT to 0x00.

BUCK.VOUT Register Value	V _{LOAD} [V]
0x00	OFF
0x01	0.6
0x02	0.9
0x03	1.2
0x04	1.5
0x05	1.8
0x06	2.2
0x07	2.5 ¹

Table 37: V_{LOAD} settings by BUCK.VOUT register

- This configuration is only available if V_{OVDIS} ≥ 2.5 V.



9.7. Temperature Monitoring Enable (TMON)

This register is used to enable/disable thermal monitoring described in Sections 9.8 and 9.9.

TMON Register	0x0F	R/W
	Bit [7:1]	Bit [0]
RESERVED		EN
0x00		1

Table 38: TMON register

9.8. STO Charge Temperature Monitoring (TEMPCOLDCH and TEMPHOTCH)

Those fields are used to configure the minimum (cold) and maximum (hot) temperature thresholds for charging the battery on [STO](#).

THRESH value is determined as follows from the desired temperature T:

- Determine the resistance of the thermo resistor R_{TH} at the desired temperature.

Bit [0]: EN (TMON.EN).

This field is used to enable the temperature monitoring:

- 0: DIS - Disable the temperature monitoring.
- 1: EN - Enable the temperature monitoring

- Calculate THRESH using the following formula:

$$THRESH = \frac{256 \cdot R_{TH}}{R_{DIV} + R_{TH}}$$

See Section 6.7 for further information about thermal monitoring configuration.

9.8.1. TEMPCOLDCH

Minimum temperature for storage element charging register.

TEMPCOLDCH Register	0x0B	R/W
	Bit [7:0]	
THRESH		
0xD1		

Table 39: TEMPCOLDCH register

9.8.2. TEMPHOTCH

Maximum temperature for storage element charging register.

TEMPHOTCH Register	0x0C	R/W
	Bit [7:0]	
THRESH		
0x18		

Table 40: TEMPHOTCH register

Bit [7:0]: THRESH (TEMPCOLDCH.THRESH).

This field is used to configure the minimum temperature (cold) threshold.

Bit [7:0]: THRESH (TEMPHOTCH.THRESH).

This field is used to configure the maximum temperature (hot) threshold.



9.9. STO Discharge Temperature Monitoring (TEMPCOLDDIS and TEMPHTODIS)

Those fields are used to configure the minimum (cold) and maximum (hot) temperature thresholds for discharging the battery on [STO](#).

See Section 6.7 for further information about thermal monitoring configuration.

9.9.1. TEMPCOLDDIS

Minimum temperature (cold) for storage element discharging register.

TEMPCOLDDIS Register	0x0D	R/W
	Bit [7:0]	
	THRESH	
	0xD1	

Table 41: TEMPCOLDDIS register

9.9.2. TEMPHTODIS

Maximum temperature (hot) for storage element discharging register.

TEMPHTODIS Register	0x0E	R/W
	Bit [7:0]	
	THRESH	
	0x18	

Table 42: TEMPHTODIS register

Bit [7:0]: THRESH (TEMPCOLDDIS.THRESH).

This fields is used to configure the minimum temperature (cold) threshold.

Bit [7:0]: THRESH (TEMPHTODIS.THRESH).

This fields is used to configure the maximum temperature (hot) threshold.



9.10. Source Low Threshold (SRCLOW)

Configures the V_{SRCLOW} threshold, which is the $SRCx$ voltage threshold below which the AEM13920 switches to **SLEEP STATE**.

SRCLOW Register		0x10	R/W
Bit [7:6]	Bit [5:3]	Bit [2:0]	
RESERVED	SRC2THRESH	SRC1THRESH	
0x00	0x00	0x00	

Table 43: SRCLOW register

Bit [5:3]: SRC2THRESH (SRCLOW.SRC2THRESH).

This field is used to configure the V_{SRCLOW} threshold of $SRC2$.

Bit [2:0]: SRC1THRESH (SRCLOW.SRC1THRESH).

This field is used to configure the V_{SRCLOW} threshold of $SRC1$.

Table 44 shows the threshold voltages V_{SRCLOW} according to the configuration of SRCLOW.SRCxTHRESH fields:

SRCxTHRESH	Source Low Voltage Threshold V_{SRCLOW} [V]
0x00	0.113
0x01	0.203
0x02	0.255
0x03	0.300
0x04	0.360
0x05	0.405
0x06	0.510
0x07	0.600

Table 44: V_{SRCLOW} thresholds as configured by the SRCLOW register



9.11. IRQ Enable (IRQENx)

9.11.1. IRQENO

IRQ pin event enable register 0: configures on which event the IRQ pin shows a rising edge (see also the IRQEN1 register).

IRQENO Register								0x12	R/W
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]		
RESERVED	TEMPDIS	TEMPCH	SRCLOW	VOVCH	VCHRDY	VOVDIS	I2CRDY		
0	0	0	0	0	0	0	1		

Table 45: IRQENO register

Bit [6]: TEMPDIS (IRQENO.TEMPDIS).

Setting this bit enables or disables the generation of a rising edge on the IRQ pin when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers).

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [5]: TEMPCH (IRQENO.TEMPCH).

Setting this bit enables or disables the generation of a rising edge on the IRQ pin when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers).

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [4]: SRCLOW (IRQENO.SRCLOW).

Setting this bit enables or disables the generation of a rising edge on the IRQ pin when both sources cross the V_{SRCLOW} threshold (selected through the SRCLOW.SRCxTHRESH fields).

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [3]: VOVCH (IRQENO.VOVCH).

Setting this bit enables or disables the generation of a rising edge on the IRQ pin when the storage element voltage crosses the overcharge threshold (selected through the VOVCH register).

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [2]: VCHRDY (IRQENO.VCHRDY).

Setting this bit enables or disables the generation of a rising edge on the IRQ pin when the storage element voltage crosses the ready threshold (selected through the VCHRDY register).

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [1]: VOVDIS (IRQENO.VOVDIS).

Setting this bit enables or disables the generation of a rising edge on the IRQ pin when the storage element voltage crosses the overdischarge threshold (selected through the VOVDIS register).

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [0]: I2CRDY (IRQENO.I2CRDY).

Setting this bit enables or disables the generation of a rising edge on the IRQ pin when the serial interface (I²C) is ready to communicate.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.



9.11.2. IRQEN1

IRQ pin event enable register 1: configures on which event the **IRQ** pin shows a rising edge (see also the IRQENO register).

IRQEN1 Register							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
APMERR	APMDONE	TEMPDONE	STODONE	SRC2MPPTDONE	SRC2MPPTSTART	SRC1MPPTDONE	SRC1MPPTSTART
0	0	0	0	0	0	0	0

Table 46: IRQEN1 register

Bit [7]: APMERR (IRQENO.APMERR).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when a APM (BUCK) error occurs.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [6]: APMDONE (IRQENO.APMDONE).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when APM data is available.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [5]: TEMPDONE (IRQENO.TEMPDONE).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when the temperature ADC is done.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [4]: STODONE (IRQENO.STODONE).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when the STO ADC is done.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [3]: SRC2MPPTDONE (IRQENO.SRC2MPPTDONE).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when the MPPT (source 2) is done.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [2]: SRC2MPPTSTART (IRQENO.SRC2MPPTSTART).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when the MPPT (source 2) starts.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [1]: SRC1MPPTDONE (IRQENO.SRC1MPPTDONE).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when the MPPT (source 1) is done.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.

Bit [0]: SRC1MPPTSTART (IRQENO.SRC1MPPTSTART).

Setting this bit enables or disables the generation of a rising edge on the **IRQ** pin when the MPPT (source 1) starts.

- 0: DIS - Disable the event.
- 1: EN - Enable the event.



9.12. IRQ Flags (IRQFLGx)

The IRQFLGx registers allow users to get a status about specific AEM13920 events. When the event happens, the **IRQ** pin switches HIGH and the register field bit that corresponds to the event will switch to 1, provided that the event flag has been enabled in the corresponding IRQENx register. The bit will stay to 1 and the **IRQ** pin will stay HIGH until the IRQFLGx register is read.

9.12.1. IRQFLG0

IRQ pin event flags register 0.

IRQFLG0 Register								0x15	R
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]		
RESERVED	TEMPDIS	TEMPCH	SRCLOW	VOVCH	VCHRDY	VOVDIS	I2CRDY		
0	0	0	0	0	0	0	1		

Table 47: IRQFLG0 register

Bit [6]: TEMPDIS (IRQFLG0.TEMPDIS).

This **IRQ** pin event flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [5]: TEMPCH (IRQFLG0.TEMPCH).

This **IRQ** pin event flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [4]: SRCLOW (IRQFLG0.SRCLOW).

This **IRQ** pin event flag is set when both sources cross the V_{SRCLOW} threshold (selected through the SRCLOW.SRCxTHRESH fields), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Please note that if the AEM13920 is configured through the I²C registers to enable IRQ flags, the behavior of the **IRQ** pin as well as the IRQFLGx register stays the same even if the AEM13920 has switched back to GPIO configuration by writing 0 to CTRL.UPDATE.

Bit [3]: VOVCH (IRQFLG0.VOVCH).

This **IRQ** pin event flag is set when the storage element voltage crosses the overcharge threshold (selected through the VOVCH register), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [2]: VCHRDY (IRQFLG0.VCHRDY).

This **IRQ** pin event flag is set when the storage element voltage crosses the ready threshold (selected through the VCHRDY register), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [1]: VOVDIS (IRQFLG0.VOVDIS).

This **IRQ** pin event flag is set when the storage element voltage crosses the overdischarge threshold (selected through the VOVDIS register), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [0]: I2CRDY (IRQFLG0.I2CRDY).

This **IRQ** pin event flag is set when the serial interface (I²C) is ready to communicate, if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.



9.12.2. IRQFLG1

IRQ pin event flags register 1.

IRQFLG1 Register								0x16	R
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]		
APMERR	APMDONE	TEMPDONE	STODONE	SRC2MPPTDONE	SRC2MPPTSTART	SRC1MPPTDONE	SRC1MPPTSTART		
0	0	0	0	0	0	0	0		

Table 48: IRQFLG1 register

Bit [7]: APMERR (IRQENO.APMERR).

This IRQ pin event flag is set when a APM (BUCK) error occurs, if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [6]: APMDONE (IRQENO.APMDONE).

This IRQ pin event flag is set when APM data is available, if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [5]: TEMPDONE (IRQENO.TEMPDONE).

This IRQ pin event flag is set when the temperature ADC is done, if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [4]: STODONE (IRQENO.STODONE).

This IRQ pin event flag is set when the STO ADC is done, if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [3]: SRC2MPPTDONE (IRQENO.SRC2MPPTDONE).

This IRQ pin event flag is set when the MPPT is done (source 2), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [2]: SRC2MPPTSTART (IRQENO.SRC2MPPTSTART).

This IRQ pin event flag is set when the MPPT starts (source 2), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [1]: SRC1MPPTDONE (IRQENO.SRC1MPPTDONE).

This IRQ pin event flag is set when the MPPT is done (source 1), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.

Bit [0]: SRC1MPPTSTART (IRQENO.SRC1MPPTSTART).

This IRQ pin event flag is set when the MPPT starts (source 1), if the corresponding event source has been previously enabled.

- 0: NFLG - Event did not occur.
- 1: FLG - Event occurred.



9.13. Status (STATUSx)

9.13.1. STATUS0

Status 0 register.

STATUS0 Register		0x17				R
Bit [7:5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	
RESERVED	SRC2SRCLOW	SRC1SRCLOW	VOVCH	VCHRDY	VOVDIS	
0x00	0	0	0	0	0	

Table 49: STATUS0 register

Bit [4]: SRC2SRCLOW (STATUS0.SRC2SRCLOW).

This status indicates whether the source is higher than the V_{SRCLOW} level or not.

- 0: HIGH - The source is higher than the V_{SRCLOW} level
- 1: LOW - The source is lower than the V_{SRCLOW} level

Bit [3]: SRC1SRCLOW (STATUS0.SRC1SRCLOW).

This status indicates whether the source is higher than the V_{SRCLOW} level or not.

- 0: HIGH - The source is higher than the V_{SRCLOW} level
- 1: LOW - The source is lower than the V_{SRCLOW} level

9.13.2. STATUS1

Status 1 register.

STATUS1 Register		0x18				R
Bit [7:4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]		
RESERVED	TEMPHOTDIS	TEMPCOLDDIS	TEMPHOTCH	TEMPCOLDCH		
0x00	0	0	0	0		

Table 50: STATUS1 register

Bit [3]: TEMPHOTDIS (STATUS1.TEMPHOTDIS).

This status indicates whether the temperature is higher than the hot threshold (for storage element discharging) or not.

- 0: LOW - Temperature is below the hot threshold.
- 1: HIGH - Temperature is above the hot threshold.

Bit [2]: VOVCH (STATUS0.VOVCH).

This status indicates whether the storage element voltage is higher than the overcharge level or not.

- 0: LOW - The storage element voltage is lower than the overcharge level.
- 1: HIGH - The storage element voltage is higher than the overcharge level.

Bit [1]: VCHRDY (STATUS0.VCHRDY).

This status indicates whether the storage element voltage is higher than the ready level or not.

- 0: LOW - The storage element voltage is lower than the ready level.
- 1: HIGH - The storage element voltage is higher than the ready level.

Bit [0]: VOVDIS (STATUS0.VOVDIS).

This status indicates whether the storage element voltage is higher than the overdischarge level or not.

- 0: LOW - The storage element voltage is higher than the overdischarge level.
- 1: HIGH - The storage element voltage is lower than the overdischarge level.

Bit [2]: TEMPCOLDDIS (STATUS1.TEMPCOLDDIS).

This status indicates whether the temperature is higher than the cold threshold (for storage element discharging) or not.

- 0: HIGH - Temperature is above the cold threshold.
- 1: LOW - Temperature is below the cold threshold.

Bit [1]: TEMPHOTCH (STATUS1.TEMPHOTCH).

This status indicates whether the temperature is higher than the hot threshold (for storage element charging) or not.

- 0: LOW - Temperature is below the hot threshold.
- 1: HIGH - Temperature is above the hot threshold.

Bit [0]: TEMPCOLDCH (STATUS1.TEMPCOLDCH).

This status indicates whether the temperature is higher than the cold threshold (for storage element charging) or not.

- 0: HIGH - Temperature is above the cold threshold.
- 1: LOW - Temperature is below the cold threshold.



9.14. Average Power Monitoring Configuration (APM)

APM configuration register. The configuration of this register affects the APM readings of both boost converters, as well as the readings of the buck converter.

APM Register		0x11		R/W	
Bit [7:5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	RSVD 2	RSVD 1	BUCKEN	SRC2EN	SRC1EN
0x00	0	0	0	0	0

Table 51: APM register

Bit [4]: Reserved 2 (APM.RSVD2).

Always write 0x00 to this register when the APM is used.

Bit [3]: Reserved 1 (APM.RSVD1).

Always write 0x01 to this register when the APM is used.

Bit [2]: BUCKEN (APM.BUCKEN).

This field is used to enable the APM for BUCK.

- 0: DIS - Disable the APM.
- 1: EN - Enable the APM.

Bit [1]: SRC2EN (APM.SRC2EN).

This field is used to enable the APM for SRC2.

- 0: DIS - Disable the APM.
- 1: EN - Enable the APM.

Bit [0]: SRC1EN (APM.SRC1EN).

This field is used to enable the APM for SRC1.

- 0: DIS - Disable the APM.
- 1: EN - Enable the APM.



9.15. SRCx APM Data (APMxSRCx)

9.15.1. APM0SRCx

APM data 0 register ([SRCx](#)).

APM0SRC1 Register	0x19	R
APM0SRC2 Register	0x1C	R
Bit [7:0]		
DATA		
0x00		

Table 52: APM0SRCx register

9.15.2. APM1SRCx

APM data 1 register ([SRCx](#)).

APM1SRC1 Register	0x1A	R
APM1SRC2 Register	0x1D	R
Bit [7:0]		
DATA		
0x00		

Table 53: APM1SRCx register

9.15.3. APM2SRCx

APM data 2 register ([SRCx](#)).

APM2SRC1 Register	0x1B	R
APM2SRC2 Register	0x1E	R
Bit [7]		
Bit [6:0]		
RESERVED		
DATA		
0x00	0x00	

Table 54: APM2SRCx register

Bit [7:0]: DATA (APM0SRCx.DATA).

This register contains the bits [7:0] of the SRCx APM data.

Bit [7:0]: DATA (APM1SRCx.DATA).

This register contains the bits [15:8] of the SRCx APM data.

Bit [6:0]: DATA (APM2SRCx.DATA).

This register contains the bits [22:16] of the SRCx APM data.



9.16. BUCK APM Data (APMxBUCK)

9.16.1. APM0BUCK

APM data 0 register (BUCK).

Bit [7:0]: DATA (APM0BUCK.DATA).

APM0BUCK Register	0x1F	R
Bit [7:0]		
DATA		
	0x00	

Table 55: APM0BUCK register

9.16.2. APM1BUCK

APM data 1 register (BUCK).

Bit [7:0]: DATA (APM1BUCK.DATA).

APM1BUCK Register	0x20	R
Bit [7:0]		
DATA		
	0x00	

Table 56: APM1BUCK register

9.16.3. APM2BUCK

APM data 2 register (BUCK).

Bit [6:0]: DATA (APM2BUCK.DATA).

APM2BUCK Register	0x21	R
Bit [7]	Bit [6:0]	
RESERVED		
0	0x00	

Table 57: APM2BUCK register



9.17. APM Error (APMERR)

APM errors status register.

APMERR Register		0x22			R		
Bit [7:6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	
RESERVED	BUCKNVLD	BUCKERR	SRC2NVLD	SRC2ERR	SRC1NVLD	SRC1ERR	
0x00	0	0	0	0	0	0	

Table 58: APMERR register

Bit [5]: BUCKNVLD (APMERR.BUCKNVLD).

This field indicates whether the BUCK data is corrupted or not.

- 0: OK - The BUCK data is valid.
- 1: ERR - The BUCK data is corrupted.

Bit [4]: BUCKERR (APMERR.BUCKERR).

This field indicates whether a BUCK error occurred or not.

- 0: OK - No BUCK error occurred.
- 1: ERR - A BUCK error occurred

Bit [3]: SRC2NVLD (APMERR.SRC2NVLD).

This field indicates whether the SRC2 data is corrupted or not.

- 0: OK - The SRC2 data is valid.
- 1: ERR - The SRC2 data is corrupted.

Bit [2]: SRC2ERR (APMERR.SRC2ERR).

This field indicates whether a SRC2 error occurred or not.

- 0: OK - No SRC2 error occurred.
- 1: ERR - A SRC2 error occurred.

Bit [1]: SRC1NVLD (APMERR.SRC1NVLD).

This field indicates whether the SRC1 data is corrupted or not.

- 0: OK - The SRC1 data is valid
- 1: ERR - The SRC1 data is corrupted

Bit [0]: SRC1ERR (APMERR.SRC1ERR).

This field indicates whether a SRC1 error occurred or not.

- 0: OK - No SRC1 error occurred
- 1: ERR - A SRC1 error occurred



9.18. Temperature Monitoring Data (TEMP)

Temperature monitoring data register.

TEMP Register	0x23	R
	Bit [7:0]	
	DATA	
	0x00	

Table 59: TEMP register

Bit [7:0]: DATA (TEMP.DATA).

This field gives the code that results from the ADC acquisition for the temperature monitoring.

R_{TH} can be determined using the following equation:

$$R_{TH} = \frac{R_{DIV} \cdot DATA}{256 - DATA}$$

Thus the temperature T in Kelvin can be obtained with the following formula.

$$T = \frac{B}{\ln\left(\frac{R_{TH}}{R_0}\right) + \frac{B}{T_0}}$$

See Section 5.4 for further information.

9.19. Storage Element Voltage Data (STO)

Storage monitoring register.

STO Register	0x24	R
	Bit [7:0]	
	DATA	
	0x00	

Table 60: STO register

Bit [7:0]: DATA (STO.DATA).

This field contains the code that results from the ADC acquisition for the storage monitoring. V_{STO} can be determined using the following formula:

$$V_{STO} = \frac{4.8 \cdot DATA}{256}$$



9.20. Sources Voltage Data (SRCx)

Source data registers (SRC1 and SRC2).

To convert data from the register to Volts, use either the formulas from Table 62 or the values from Table 63 used as a lookup table. Please note that values in register SRCx.DATA are always within the ranges given in those two tables.

SRC1 Register	0x25	R
SRC2 Register	0x26	R
Bit [7:0]		
DATA		
0x00		

Table 61: SRCx register

SRCx.DATA Range	Formula [V]
0x00 - 0x06	0.113
0x07 - 0x12	$0.09 + (2 \cdot \text{DATA} - 9) \cdot 0.0075$
0x13 - 0x39	$0.3 + (2 \cdot \text{DATA} - 37) \cdot 0.015$
0x68 - 0x79	$\frac{0.3 + (2 \cdot \text{DATA} - 165) \cdot 0.015}{0.67}$
0x9F - 0xB9	$\frac{0.3 + (2 \cdot \text{DATA} - 293) \cdot 0.015}{0.33}$

Table 62: Source voltage V_{SRCx} from SRCx.DATA register value (formula)

Bit [7:0]: DATA (SRCx.DATA).

This field contains the code that results from the ADC acquisition for the MPPT regulation. Maximum value is 0xB9.

SRCx.DATA [7:0]	V_{SRCx} [V]	SRCx.DATA [7:0]	V_{SRCx} [V]
0x00	0.113	0x1D	0.615
...	...	0x1E	0.645
0x06	0.113	0x1F	0.675
0x07	0.128	0x20	0.705
0x08	0.143	0x21	0.735
0x09	0.158	0x22	0.765
0x0A	0.173	0x23	0.795
0x0B	0.188	0x24	0.825
0x0C	0.203	0x25	0.855
0x0D	0.218	0x26	0.885
0x0E	0.233	0x27	0.915
0x0F	0.248	0x28	0.945
0x10	0.263	0x29	0.975
0x11	0.278	0x2A	1.005
0x12	0.293	0x2B	1.035
0x13	0.315	0x2C	1.065
0x14	0.345	0x2D	1.095
0x15	0.375	0x2E	1.125
0x16	0.405	0x2F	1.155
0x17	0.435	0x30	1.185
0x18	0.465	0x31	1.215
0x19	0.495	0x32	1.245
0x1A	0.525	0x33	1.275
0x1B	0.555	0x34	1.305
0x1C	0.585	0x35	1.335

SRCx.DATA [7:0]	V_{SRCx} [V]	SRCx.DATA [7:0]	V_{SRCx} [V]
0x36	1.365	0xA2	2.318
0x37	1.395	0xA3	2.409
0x38	1.425	0xA4	2.500
0x39	1.455	0xA5	2.591
0x68	1.410	0xA6	2.682
0x69	1.455	0xA7	2.773
0x6A	1.500	0xA8	2.864
0x6B	1.545	0xA9	2.955
0x6C	1.590	0xAA	3.045
0x6D	1.634	0xAB	3.136
0x6E	1.679	0xAC	3.227
0x6F	1.724	0xAD	3.318
0x70	1.769	0xAE	3.409
0x71	1.813	0xAF	3.500
0x72	1.858	0xB0	3.591
0x73	1.903	0xB1	3.682
0x74	1.948	0xB2	3.773
0x75	1.993	0xB3	3.864
0x76	2.037	0xB4	3.955
0x77	2.082	0xB5	4.045
0x78	2.127	0xB6	4.136
0x79	2.172	0xB7	4.227
0x9F	2.045	0xB8	4.318
0xA0	2.136	0xB9	4.409
0xA1	2.227		

Table 63: Source voltage V_{SRCx} from SRCx.DATA register value (lookup table)



10. Typical Application Circuits

10.1. Example Circuit 1

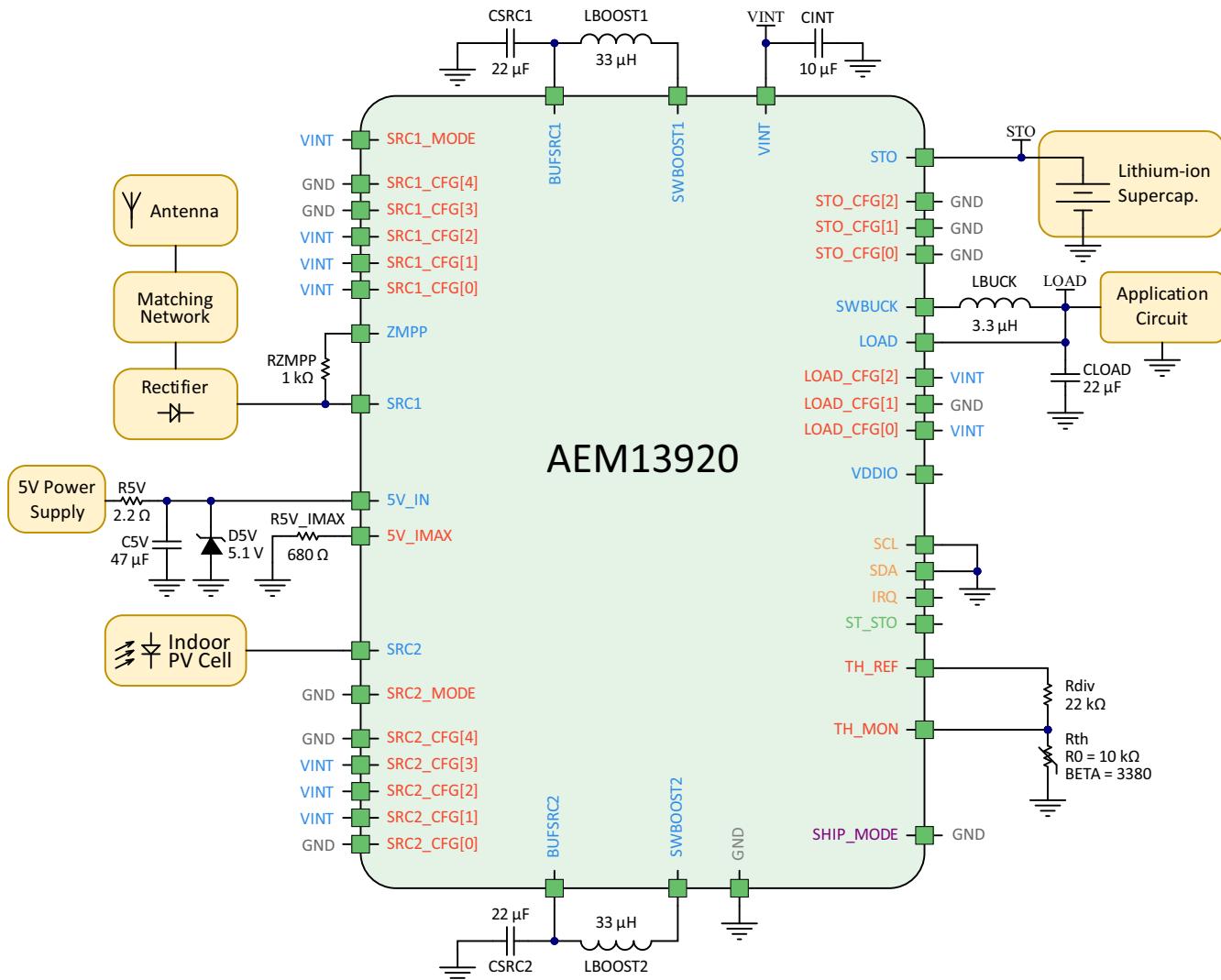


Figure 13: Typical application circuit 1

Figure 13 shows a typical application circuit of the AEM13920.

Configuration of SRC1

The first energy source is a RF harvester (antenna, matching network and RF rectifier), which has been optimized to provide maximum power when loaded with $1\text{ k}\Omega$. The fastest sampling/period is set to ensure maximum reactivity, as RF signal level is likely to change quickly.

- $\text{SRC1_MODE} = \text{H}$ (MPPT).
- $\text{SRC1_CFG[2:0]} = \text{HHH}$ (ZMPP mode).
- $\text{SRC1_CFG[4:3]} = \text{LL}$.
 - $T_{\text{MPPT,SAMPLING}} = 2\text{ ms}$.
 - $T_{\text{MPPT,PERIOD}} = 128\text{ ms}$.

- $R_{\text{ZMPP}} = 1\text{ k}\Omega$.
- $L_{\text{BOOST1}} = 33\text{ }\mu\text{H}$ for a good tradeoff between efficiency and maximum current with default boost timing when I^2C is not used (see Sections 6.5 and 9.5).

Configuration of SRC2

The second energy source is an indoor PV cell which has a constant 0.75 V MPP voltage. SRC2 is configured as follows:

- $\text{SRC2_MODE} = \text{L}$ (constant voltage).
- $\text{SRC2_CFG[4:0]} = \text{LHHHL}$ (0.75 V regulation).
- $L_{\text{BOOST2}} = 33\text{ }\mu\text{H}$.



Configuration of STO

The storage element is a Lithium-ion supercapacitor, so storage element threshold voltages are set as follows:

- $\text{STO_CFG[2:0]} = \text{LLL}$.
- $V_{\text{OVDIS}} = 2.50 \text{ V}$.
- $V_{\text{CHRDY}} = 2.55 \text{ V}$.
- $V_{\text{OVCH}} = 3.80 \text{ V}$.

Configuration of LOAD

The application circuit is supplied with 1.8 V with current peaks up to 100 mA. The buck converter is configured as follows:

- $\text{LOAD_CFG[2:0]} = \text{HLH} (1.8 \text{ V})$.
- $L_{\text{BUCK}} = 3.3 \mu\text{H}$ for high current capability.

Configuration of 5V_IN

The maximum allowed current to charge the storage element is 75 mA. Closest standard series resistor is 680Ω , which leads to a 73.5 mA maximum current.

- $R_{5V_IMAX} = 680 \Omega$.
- $I_{5V,CC} = 73.5 \text{ mA}$.

The RC filter, which role is to slow down the rise time of the 5 V source, can be determined with the following steps.

R_{5V} is calculated so that the voltage drop across it ensures a voltage on $5V_IN$ higher than $V_{\text{OVCH}} + 200 \text{ mV}$:

$$I_{5V,CC} \cdot R_{5V} < 5V - V_{\text{OVCH}} - 0.2V$$

$$R_{5V} < \frac{5V - V_{\text{OVCH}} - 0.2V}{I_{5V,CC}} \Leftrightarrow R_{5V} < \frac{5V - 3.8V - 0.2V}{73.5 \times 10^{-3}}$$

$$R_{5V} < 13.6\Omega$$

C_{5V} is calculated so that the $5V_IN$ voltage rise time remains below $T_{5V,RISE}$:

$$R_{5V} \cdot C_{5V} > T_{5V,RISE}$$

$$R_{5V} \cdot C_{5V} > 50\mu\text{s}$$

To meet these two conditions, the following component values have been selected:

- $R_{5V} = 2.2 \Omega$
- $C_{5V} = 47 \mu\text{F}$

The 5 V source is expected to have ripple and/or over voltages up to 5.5 V, so a 5.1 V zener diode D_{5V} is added to prevent those to damage the AEM13920.

The minimum required power rating of D_{5V} is computed as follows, from its maximum reverse current I_{D5V} , its voltage V_{D5V} and the resistor R_{5V} :

$$P_{D5V} \geq I_{D5V} \cdot V_{D5V} \Leftrightarrow P_{D5V} \geq \frac{5.5V - 5.1V}{R_{5V}} \cdot 5.1V$$

$$P_{D5V} \geq \frac{5.5V - 5.1V}{2.2} \cdot 5.1V \Leftrightarrow P_{D5V} \geq 927\text{mW}$$

R_{5V} dissipated power $P_{R5V,idle}$ when the 5 V charger does not pull any current to charge the storage element is determined as follows:

$$P_{R5V,idle} = \frac{(5.5V - 5.1V)^2}{R_{5V}} \Leftrightarrow P_{R5V,idle} = \frac{(5.5V - 5.1V)^2}{2.2}$$

$$P_{R5V,idle} = 73\text{mW}$$

Furthermore, R_{5V} dissipated power $P_{R5V,CC}$ at $I_{5V,CC}$ current (73.5 mA) is determined as follows:

$$P_{R5V,CC} = R_{5V} \cdot I_{5V,CC}^2 = 2.2\Omega \cdot (73.5\text{mA})^2 = 12\text{mW}$$

The minimum required power rating of R_{5V} is the maximum of $P_{R5V,idle}$ and $P_{R5V,CC}$, thus, 73 mW.

I²C configuration

I²C is not used:

- SDA and SCL are tied to GND.
- IRQ and VDDIO are left floating.

Temperature monitoring

Temperature monitoring is used to protect the storage element from being charged and discharged when temperature is outside the -25°C to +70°C range:

- R_{TH} :
- $R_0 = 10 \text{ k}\Omega$.
- $\text{BETA} = 3380$.
- $R_{DIV} = 22 \text{ k}\Omega$.

Shipping mode

Shipping mode is not used.

- SHIP_MODE is connected to GND.

10.2. Example Circuit 2

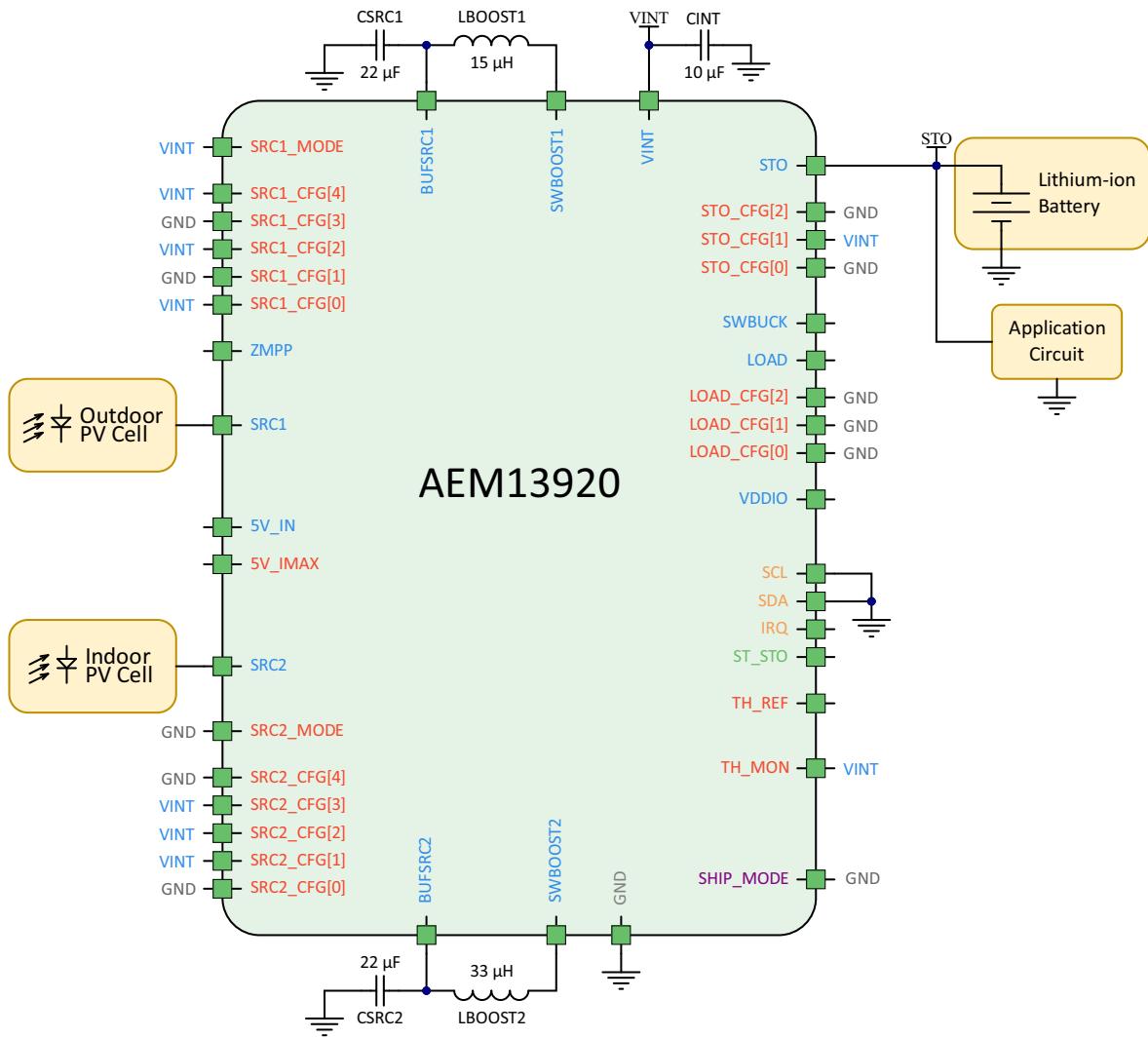


Figure 14: Typical application circuit 2

Figure 14 shows a typical application circuit of the AEM13920.

Configuration of SRC1

The first energy source is an outdoor PV cell. The MPPT is used with a 80% ratio. A medium sampling/period is set to ensure that the PV cell has enough time to reach its open circuit voltage during the V_{oc} sampling phase while still keeping a good reactivity to lighting changes.

- **SRC1_MODE** = H (MPPT).
- **SRC1_CFG[2:0]** = HLH (80%).
- **SRC1_CFG[4:3]** = HL.
 - $T_{MPPT,SAMPLING}$ = 32 ms.
 - $T_{MPPT,PERIOD}$ = 2048 ms.
- L_{BOOST1} = 15 μ H for high current capability with default boost timing when I²C is not used (see Sections 6.5 and 9.5).

Configuration of SRC2

The second energy source is an indoor PV cell which has a constant 0.75 V maximum power point voltage. [SRC2](#) is configured as follows:

- **SRC2_MODE** = L (constant voltage).
- **SRC2_CFG[4:0]** = LHHHL (0.75 V regulation).
- $L_{BOOST2} = 33 \mu\text{H}$ for a good tradeoff between efficiency and maximum current with default boost timing when I^2C is not used (see Sections 6.5 and 9.5).



Configuration of **STO**

The storage element is a Lithium-ion battery, so storage element threshold voltages are set as follows:

- **STO_CFG[2:0]** = LHL.
- V_{OVDIS} = 3.00 V.
- V_{CHRDY} = 3.30 V.
- V_{OVCH} = 4.12 V.

Configuration of **LOAD**

The application circuit is supplied from the storage element, so the **LOAD** output is not used:

- **LOAD_CFG[2:0]** = LLL: buck converter is disabled.
- **SWBUCK** and **LOAD** are left floating.

Configuration of **5V_IN**

The 5 V charger is not used:

- **5V_IN** and **5V_IMAX** are left floating.

I²C configuration

I²C is not used:

- **SDA** and **SCL** are tied to **GND**.
- **IRQ** and **VDDIO** are left floating.

Temperature monitoring

Temperature monitoring is not used:

- **TH_MON** is connected to **VINT**.
- **TH_REF** is left floating.

Shipping mode

Shipping mode is not used.

- **SHIP_MODE** is connected to **GND**.



10.3. Example Circuit 3

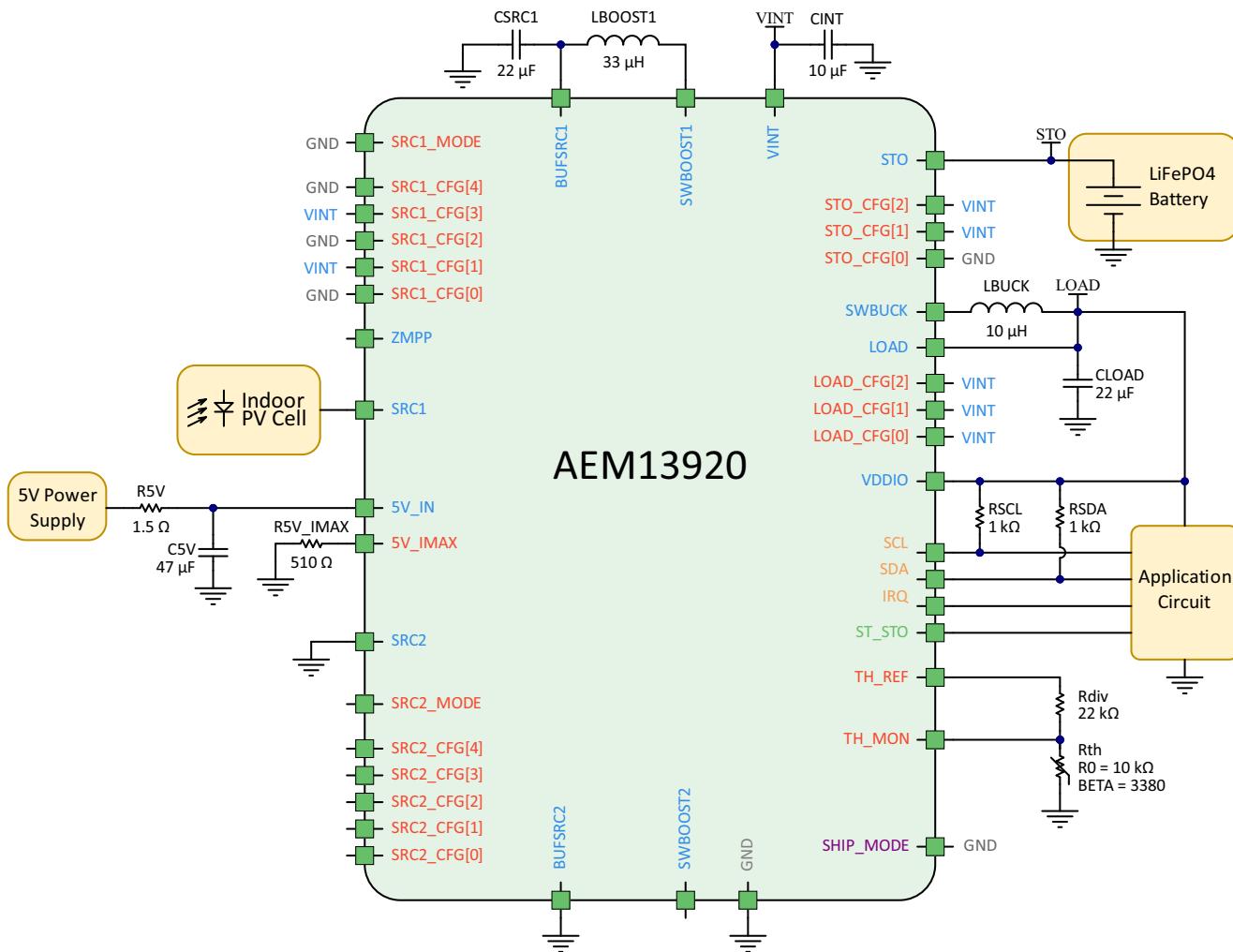


Figure 15: Typical application circuit of the AEM13920

Figure 15 shows a typical application circuit of the AEM13920.

Configuration of SRC1

The energy source is an indoor PV cell which has a constant 0.60 V maximum power point voltage. SRC1 is configured as follows:

- SRC1_MODE = L (constant voltage).
- SRC1_CFG[4:0] = LHLHL (0.60 V regulation).
- L_{BOOST1} = 33 μ H for best efficiency with default boost timing when I²C used (see Sections 6.5 and 9.5).

Configuration of SRC2

SRC2 boost converter is not used.

- SRC2, BUFSRC2 are connected to GND
- SWBOOST2 is left floating.
- SRC2_MODE and SRC2_CFG[4:0] are left floating.

Configuration of STO

The storage element is a LiFePO₄ battery, so storage element threshold voltages are set as follows:

- STO_CFG[2:0] = HHL.
- V_{OVDIS} = 2.80 V.
- V_{CHRDY} = 3.10 V.
- V_{OVCH} = 3.63 V.



Configuration of LOAD

The application circuit is supplied with 2.5 V with current peaks up to 20 mA. The buck converter is configured as follows:

- $\text{LOAD_CFG[2:0]} = \text{HHH}$ (2.5 V)
- $\text{L}_{\text{BUCK}} = 10 \mu\text{H}$ for best efficiency.
- $\text{T}_{\text{MULT}} = x2$ for best efficiency at moderate current loads (configured through I²C register, see Table 64).

Configuration of 5V_IN

The maximum allowed current to charge the storage element is 100 mA. Closest standard series resistor is 510 Ω, which leads to a 98 mA maximum current.

- $\text{R}_{\text{5V_IMAX}} = 510 \Omega$.
- $\text{I}_{\text{5V,CC}} = 98 \text{ mA}$.

The power supply connected on the 5V_IN provides a voltage from minimum 4 V to maximum 5 V. The RC filter, which role is to slow down the rise time of the 5 V source, can be selected with the following steps to ensure the 5 V charger operates properly.

R_{5V} is calculated so that the voltage drop across it ensures a voltage on 5V_IN higher than $\text{V}_{\text{OVCH}} + 200 \text{ mV}$, considering the minimum voltage from the power supply:

$$\begin{aligned} \text{I}_{\text{5V,CC}} \cdot \text{R}_{\text{5V}} &< 4\text{V} - \text{V}_{\text{OVCH}} - 0.2\text{V} \\ \text{R}_{\text{5V}} &< \frac{4\text{V} - \text{V}_{\text{OVCH}} - 0.2\text{V}}{\text{I}_{\text{5V,CC}}} \Leftrightarrow \text{R}_{\text{5V}} < \frac{4\text{V} - 3.63\text{V} - 0.2\text{V}}{98 \times 10^{-3}} \\ \text{R}_{\text{5V}} &< 1.73\Omega \end{aligned}$$

C_{5V} is calculated so that the 5V_IN voltage rise time remains below $\text{T}_{\text{5V,RISE}}$:

$$\text{R}_{\text{5V}} \cdot \text{C}_{\text{5V}} > \text{T}_{\text{5V,RISE}}$$

$$\text{R}_{\text{5V}} \cdot \text{C}_{\text{5V}} > 50\mu\text{s}$$

To meet these two conditions, the following component values have been selected:

- $\text{R}_{\text{5V}} = 1.5 \Omega$
- $\text{C}_{\text{5V}} = 47 \mu\text{F}$

R_{5V} dissipated power $\text{P}_{\text{R5V,CC}}$ at $\text{I}_{\text{5V,CC}}$ (98 mA) is determined as follows:

$$\text{P}_{\text{R5V,CC}} = \text{R}_{\text{5V}} \cdot \text{I}_{\text{5V,CC}}^2 = 1.5\Omega \cdot (98\text{mA})^2 = 14.4\text{mW}$$

I²C configuration

I²C is used to configure the AEM13920:

- VDDIO is connected to LOAD , which is the node supplying the application circuit that communicates with the AEM13920 through I²C.
- SDA and SCL are pulled-up to VDDIO with 1 kΩ resistors and connected to the application circuit micro controller (MCU) I²C bus.
- IRQ and ST_STO are connected to application circuit MCU GPIOs.

The configuration is sent through the I²C bus. Please note that the configuration done through pins (SRCx_CFG[4:0] , STO_CFG[2:0] , LOAD_CFG[2:0] , etc.) must also be written to the registers, otherwise the default register values will be applied (see Section 9 for further details about configuring the AEM13920 with I²C registers).

See Table 64 for the whole I²C register configuration (all other registers have appropriate default values).

Temperature monitoring

Temperature monitoring is used to protect the storage element from being charged and discharged outside its acceptable temperature range. The following settings are applied:

- R_{TH} :
 - $\text{R}_0 = 10 \text{ k}\Omega$.
 - $\text{BETA} = 3380$.
- $\text{R}_{\text{DIV}} = 22 \text{ k}\Omega$.
- Charging is allowed between 0°C and +45°C (see Table 64 for the values to write the registers).
- Discharging is allowed between -20°C and +65°C (see Table 64).
- Temperature monitoring is enabled by default (see Section 9.7) so it is not mandatory to write the TMON register.

Shipping mode

Shipping mode is not used.

- SHIP_MODE is connected to GND.



Register Name	Value	Notes
SRC1REGU1	0x07	Constant voltage mode.
SRC1REGU0	0x02	$V_{SRCx,REG} = 0.6$ V.
VOVDIS	0x15	$V_{OVDIS} = 2.794$ V.
VCHRDY	0x22	$V_{CHRDY} = 3.094$ V.
VOVCH	0x32	$V_{OVCH} = 3.638$ V.
BUCKCFG	0x0F	$V_{LOAD} = 2.5$ V. $T_{MULT} = 2x$.
TEMPCOLDCH	0x90	Min. 0°C for charge.
TEMPHOTCH	0x2E	Max. +45°C for charge.
TEMPCOLDDIS	0xC6	Min. -20°C for discharge.
TEMPHOTDIS	0x1B	Max. +65°C for discharge.
TMON	0x01	Enable temperature monitoring.
IRQEN1	0x40	Enable APMDONE IRQ.
CTRL	0x01	Write this register after writing the others to load I ² C register configuration.

Table 64: Summary of I²C register configuration for typical application circuit 3



11. Circuit Behavior

11.1. Start Up from SRCx

11.1.1. Configuration

- SRC1 supplied by a 2.0 V voltage source with 100 mA compliance with $700\ \Omega$ in series:
 - $V_{OC} = 2.0\ V$.
 - $V_{MPP} = 1.5\ V$ with $R_{MPPT} = 75\%$.
 - $I_{SRC1} = 714\ \mu A$.
- SRC1_MODE = H:
 - SRC1 mode is MPPT.
- SRC1_CFG[4:3] = LH:
 - $T_{MPPT,PERIOD} = 512\ ms$.
 - $T_{MPPT,SAMPLING} = 8\ ms$.
- SRC1_CFG[2:0] = HLL:
 - $R_{MPPT} = 75\%$.
- $L_{BOOST1} = 33\ \mu H$.
- STO_CFG[2:0] = LHL:
 - $V_{OVDIS} = 3.00\ V$.
 - $V_{CHRDY} = 3.30\ V$.
 - $V_{OVCH} = 4.12\ V$
- $C_{STO} = 1\ mF$ electrolytic charged at 2.8 V beforehand.
- LOAD_CFG[2:0] = HLH:
 - $V_{LOAD} = 1.8\ V$.
- $L_{BUCK} = 10\ \mu H$.
- $V_{DDIO} = 3.3\ V$ (external source).



11.1.2. Observations

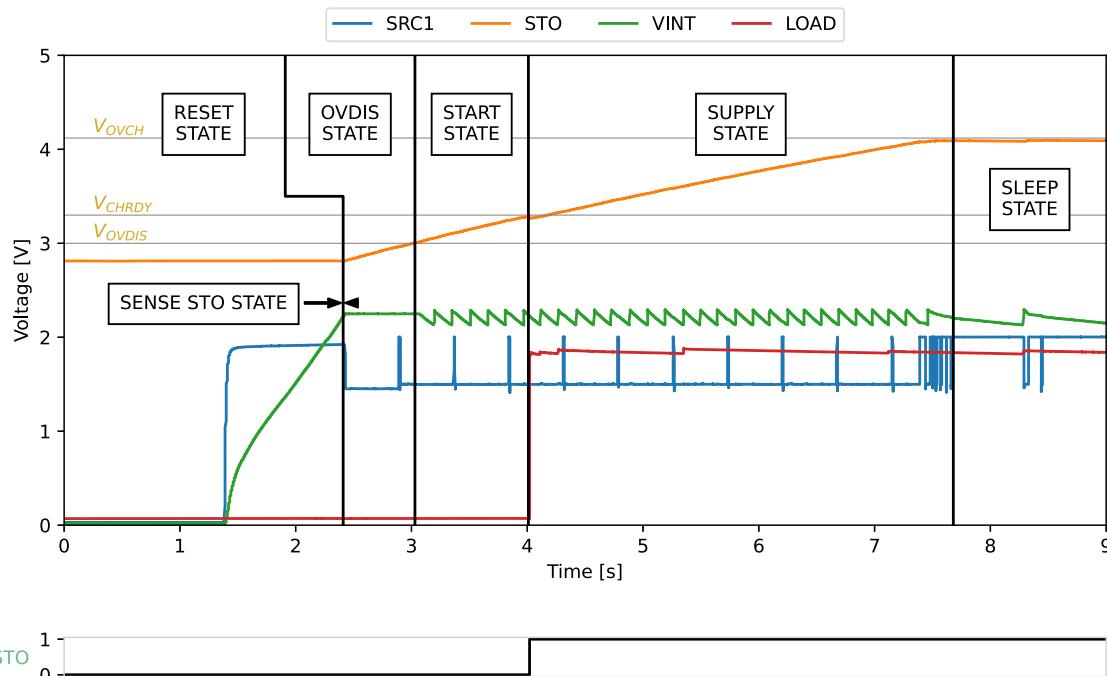


Figure 16: AEM13920 behavior at start up

- The AEM13920 is initially in **RESET STATE**.
- Once the supply connected on **SRC1** is switched on, the AEM13920 coldstarts. V_{INT} is charged until **VINT** reaches $V_{INT,CS}$. The AEM13920 switches then to **SENSE STO STATE**.
- In **SENSE STO STATE**, the AEM13920 measures V_{STO} , which is slightly below V_{OVDIS} . The AEM13920 switches then to **OVDIS STATE**.
- In **OVDIS STATE**, the AEM13920 performs a first V_{OC} evaluation and charges the storage element on **STO** by harvesting the energy from **SRC1**. V_{SRC1} is regulated at 75% of V_{OC} , thanks to the MPPT module. **VINT** is supplied by **SRC1**. Once V_{STO} reaches V_{OVDIS} , the AEM13920 switches to **START STATE**.
- In **START STATE**, the AEM13920 charges the storage element connected to **STO**. The MPPT module still ensures that V_{SRC1} is regulated at 75% of V_{OC} . The **LOAD** output remains disabled. **VINT** is supplied by **STO**. Once V_{STO} reaches V_{CHRDY} , the AEM13920 switches to **SUPPLY STATE**.
- In **SUPPLY STATE**, the AEM13920 behaves as in **START STATE** and keeps charging the storage element. The **LOAD** output is enabled, so that V_{LOAD} is regulated at 1.8 V and **ST_STO** is asserted. Once V_{STO} reaches V_{OVCH} , the AEM13920 switches to **SLEEP STATE**.
- In **SLEEP STATE**, **STO**, **LOAD** and **VINT** are fully charged. The AEM13920 stops harvesting energy from **SRC1**. Please note that around 8.3 s, the AEM13920 recharges **VINT** from **SRC1**, and around 8.5 s, the AEM13920 switches briefly to **SUPPLY STATE** to recharge **STO** from **SRC1**.



11.2. Shutdown

11.2.1. Configuration

- **SRC1** supplied by a 2.0 V voltage source with 100 mA compliance with 500 Ω in series:
 - $V_{OC} = 2.0$ V.
 - $V_{MPP} = 1.5$ V with $R_{MPPT} = 75\%$.
 - $I_{SRC1} = 1$ mA.
 - The supply is disconnected near 11.2 s.
- **SRC1_MODE** = H:
 - **SRC1** mode is MPPT.
- **SRC1_CFG[4:3]** = LH:
 - $T_{MPPT,PERIOD} = 512$ ms.
 - $T_{MPPT,SAMPLING} = 8$ ms.
- **SRC1_CFG[2:0]** = HLL:
 - $R_{MPPT} = 75\%$.
- $L_{BOOST1} = 33$ μ H.
- **STO_CFG[2:0]** = LHL:
 - $V_{OVDIS} = 3.00$ V.
 - $V_{CHRDY} = 3.30$ V.
 - $V_{OVCH} = 4.12$ V
- $C_{STO} = 10$ mF electrolytic capacitor charged at 2.8 V beforehand.
- **LOAD_CFG[2:0]** = HLH:
 - $V_{LOAD} = 1.8$ V.
 - A 200 Ω resistor is connected between **LOAD** and **GND**, so that a 9 mA current is pulled from the **LOAD** pin.
- $L_{BUCK} = 10$ μ H.
- **VDDIO** = 3.3 V (external source).



11.2.2. Observations

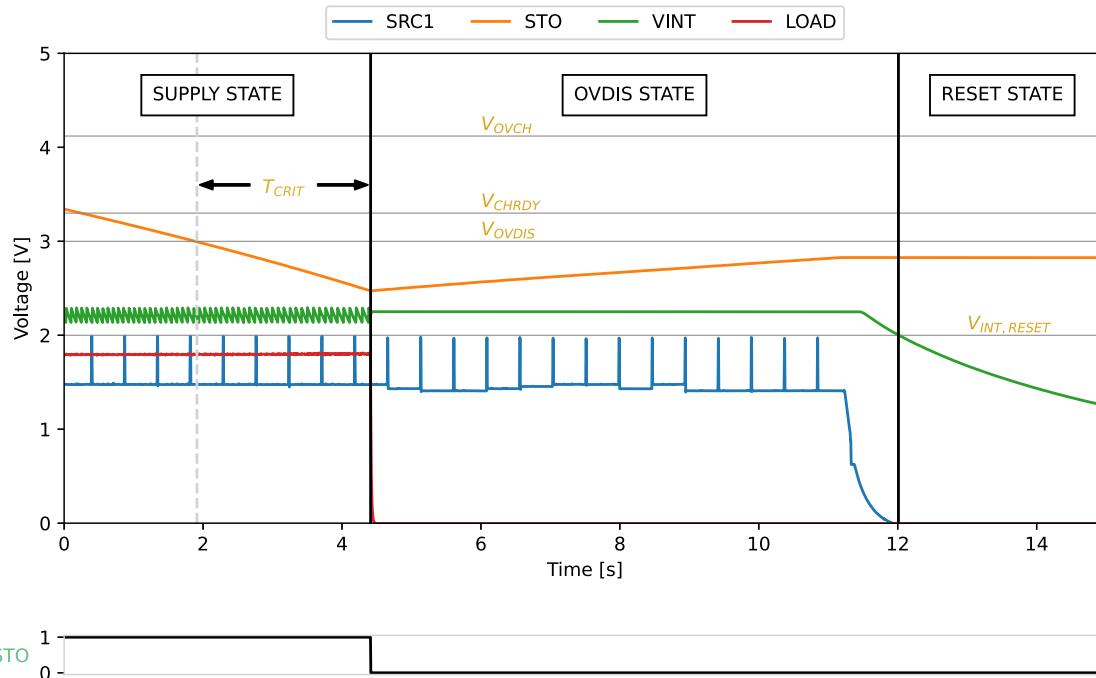


Figure 17: AEM13920 behavior at shutdown

- The AEM13920 is initially in **SUPPLY STATE**. **ST_STO** is HIGH in that state. The harvested power on **SRC1** is lower than the power supplied by **LOAD**, so that the storage element on **STO** is being discharged. Once **V_{STO}** drops below **V_{OVDIS}**, the AEM13920 stays in **SUPPLY STATE** for **T_{CRIT}** and then switches to **OVDIS STATE**.
- In **OVDIS STATE**, the **LOAD** output is disabled and **VINT** is supplied by **SRC1**. **ST_STO** is LOW in that state. There is no more current drawn on the **LOAD** pin, and thus, on the storage element on **STO**, so that the power budget is positive and the storage element is charged.
- Near 11.2 s, the power supply connected on **SRC1** is switched off. The storage element on **STO** is no longer charged, neither is **VINT**. When **V_{INT}** drops below **V_{INT,RESET}**, the AEM13920 switches to **RESET STATE**.
- In **RESET STATE**, the energy present on the storage element is preserved as the **STO** pin is set to high impedance.



11.3. Start Up from 5V_IN

11.3.1. Configuration

- $5V_{IN}$ supplied by a 5.0 V voltage source with 1 A compliance. A $370\ \Omega$ resistor is installed between $5V_{IMAX}$ and GND so that the current to charge the storage element on STO is limited to 135 mA.
- $SRCx$ are left floating.
- $STO_{CFG}[2:0] = LHL$:
 - $V_{OVDIS} = 3.00\ V$.
 - $V_{CHRDY} = 3.30\ V$.
 - $V_{OVCH} = 4.12\ V$.
- $C_{STO} = 5\ F$ supercapacitor charged at 2.8 V beforehand.
- $LOAD_{CFG}[2:0] = HLH$:
 - $V_{LOAD} = 1.8\ V$.
 - $L_{BUCK} = 10\ \mu H$.
 - $VDDIO = 3.3\ V$ (external source).

11.3.2. Observations

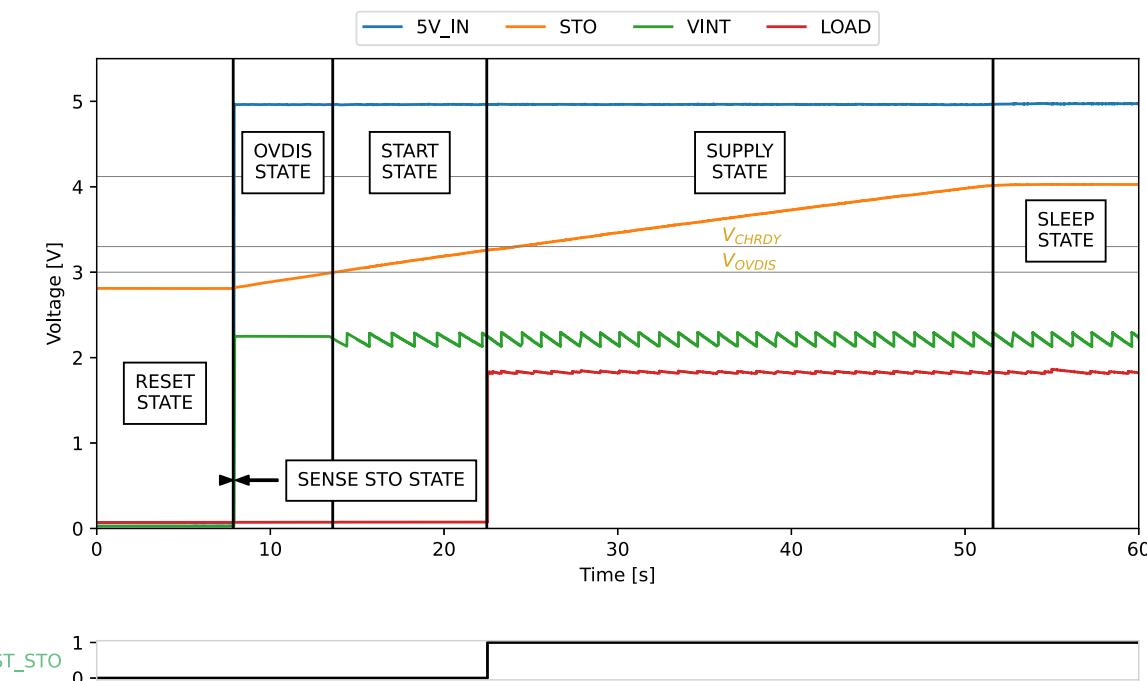


Figure 18: AEM13920 behavior at start up from 5V_IN

Observations are the same as for start up from $SRCx$ described in Section 11.1.2.

- Cold start is very fast as high power is available from $5V_{IN}$: V_{INT} rises from 0 V to 2.2 V in about 5 ms.
- The 5 F supercapacitor is charged from below V_{OVDIS} to V_{OVCH} in about 45 s. The 5 V charger circuit stops charging the storage element about 100 mV below V_{OVCH} for safety reasons.



12. Minimum BOM

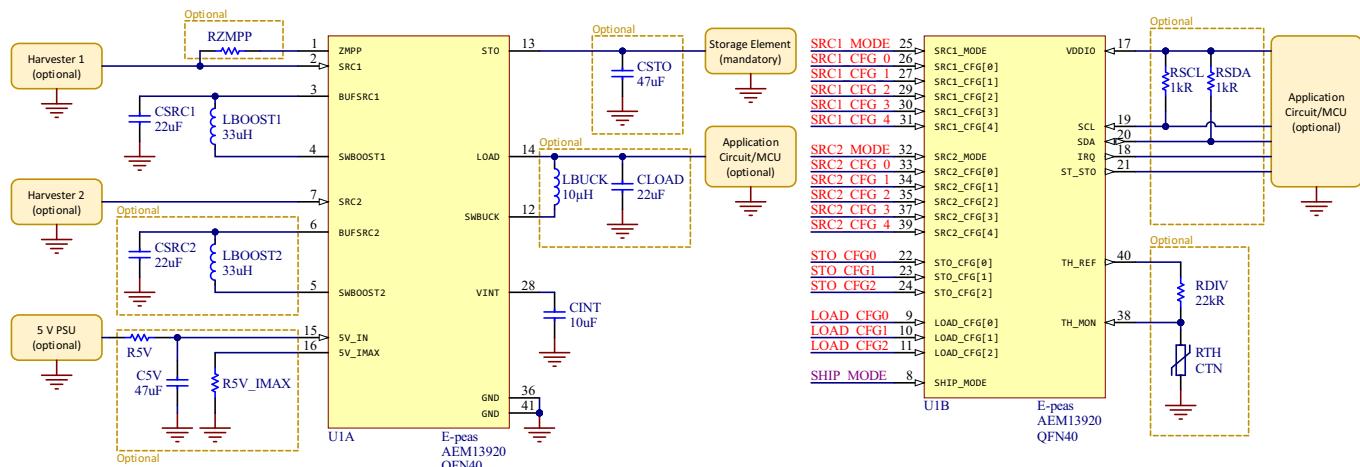


Figure 19: AEM13920 schematic

Designator	Description	Quantity	Manufacturer	Part Number
Mandatory	U1	1	e-peas	order at sales@e-peas.com
	Storage Element	1	To be defined by user.	
	CINT	1	Murata	GRM155R60J106ME44D
	CSRC1	1	Murata	GRM188R61A226ME15D
	LBOOST1	1	Coilcraft	LPS4018-333MRB
Optional	RZMPP ¹	1	To be defined by user.	
	CSRC2 ¹	1	Murata	GRM188R61A226ME15D
	LBOOST2 ¹	1	Coilcraft	LPS4018-333MRB
	C5V ¹	1	Murata	GRM188R60J476ME15D
	R5V ¹	1	To be defined by user.	
	R5V_IMAX ¹	1	To be defined by user.	
	CSTO ²	1	Murata	GRM188R60J476ME15D
	CLOAD	1	Murata	GRM188R61A226ME15D
	LBUCK	1	TDK	VLS252012CX-100M-1
	RSCL	1	Multicomp	MCWR06X1001FTL
	RSDA	1	Multicomp	MCWR06X1001FTL
	RDIV	1	Yageo	RC0402FR-0722KL
	RTH	1	Murata	NCP15XH103J03RC

Table 65: Minimum BOM

1. The AEM13920 must have at least one energy source to work: boost #1 (SRC1), boost #2 (SRC2) or 5 V input (5V_IN), or any combination of those.
2. CSTO is not mandatory but ensures high boost converter efficiency with high ESR storage elements.



13. Layout

13.1. Guidelines

Figure 20 shows an example of PCB layout with AEM13920.

The following guidelines must be applied for best performances:

- Make sure that ground and power signals are routed with large tracks. If an internal ground plane is used, place via as close as possible to the components, especially for decoupling capacitors.
- Reactive components related to the boost converters and the buck converter must be placed as close as possible to the corresponding pins ([SWBOOST_x](#), [BUFSRC_x](#), [SWBUCK](#), [LOAD](#) and [STO](#)), and be routed with large tracks/polygons.
- Keep distance between inductors to avoid magnetic coupling.
- PCB track capacitance must be reduced as much as possible on the boost converters switching nodes [SWBOOST_x](#). This is done as follows:
 - Keep the connection between the [SWBOOST_x](#)/[SWBUCK](#) pins and their corresponding inductors short.
 - Remove the ground and power planes under the [SWBOOST_x](#)/[SWBUCK](#) nodes. The polygon on the opposite external layer may also be removed.
 - Increase the distance between [SWBOOST_x](#)/[SWBUCK](#) and the ground polygon on the external PCB layer where the AEM13920 is mounted.
- PCB track capacitance must be reduced as much as possible on the [TH_REF](#) node. Same principle as for [SWBOOST_x](#) may be applied.



13.2. Example

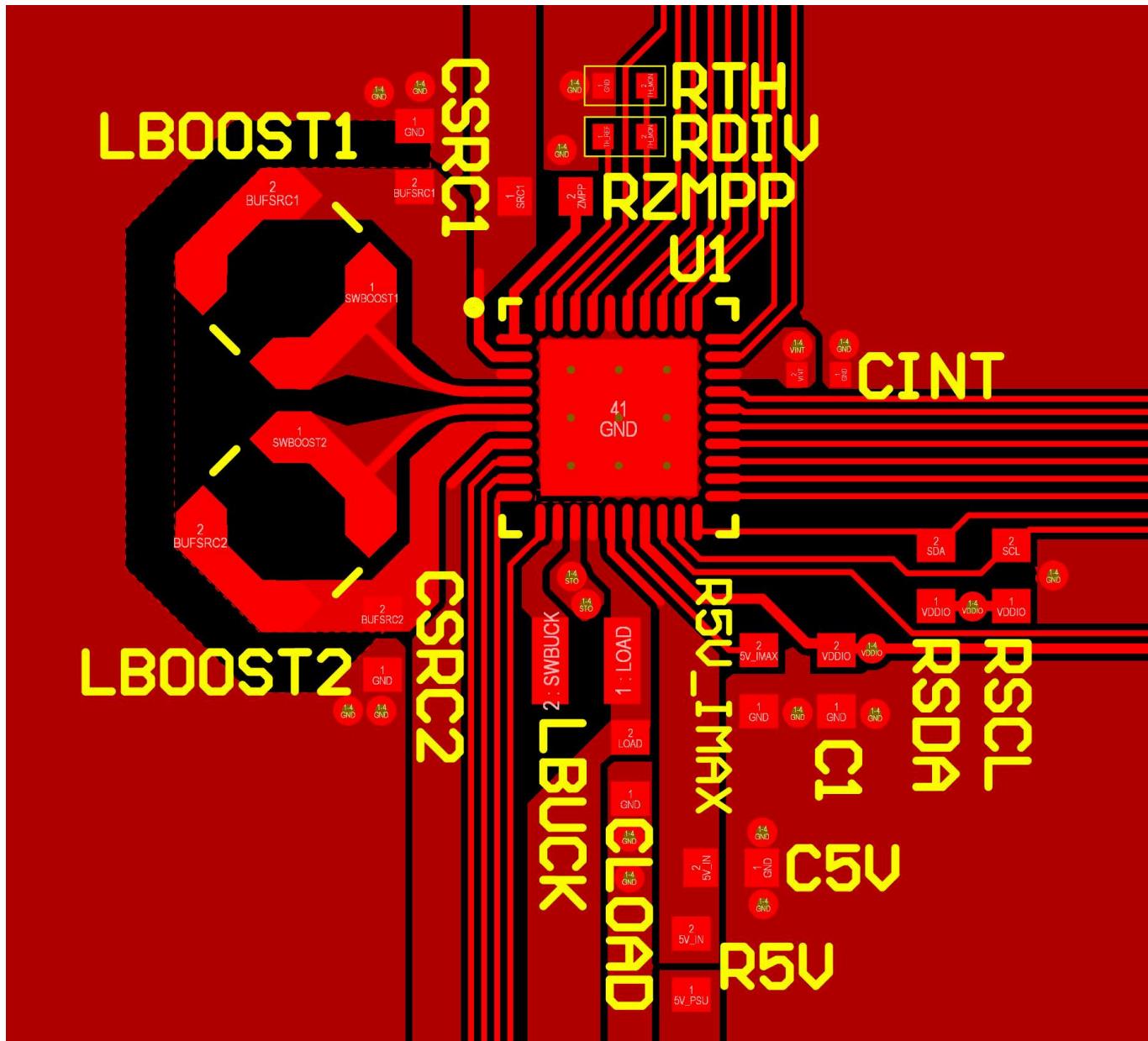


Figure 20: AEM13920 layout example



14. Package Information

14.1. Moisture Sensitivity Level

Package	Moisture Sensitivity Level (MSL) ¹
QFN-40	Level 1

Table 66: Moisture sensitivity level

1. According to JEDEC 22-A113 standard.

14.2. RoHS Compliance

e-peas product complies with RoHS requirement.

e-peas defines “RoHS” to mean that semiconductor end-products are compliant with RoHS regulation for all 10 RoHS substances.

This applies to silicon, die attached adhesive, gold wire bonding, lead frames, mold compound, and lead finish (pure tin).

14.3. REACH Compliance

The component and elements used by e-peas subcontractors to manufacture e-peas PMICs and devices are REACH compliant. For more detailed information, please contact e-peas sales team.



14.4. Package Dimensions

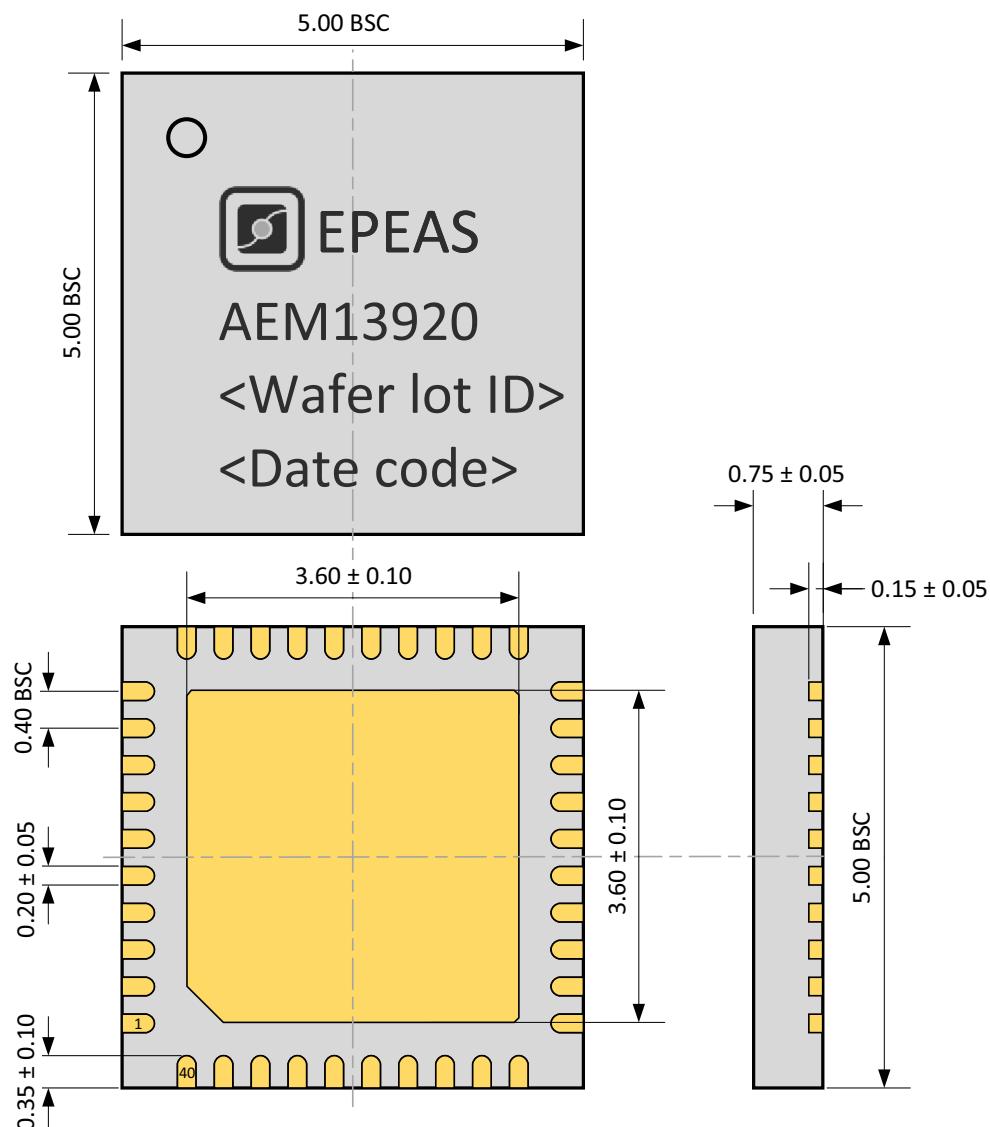


Figure 21: QFN 40-pin 5x5mm drawing (all dimensions in mm)



14.5. Board Layout

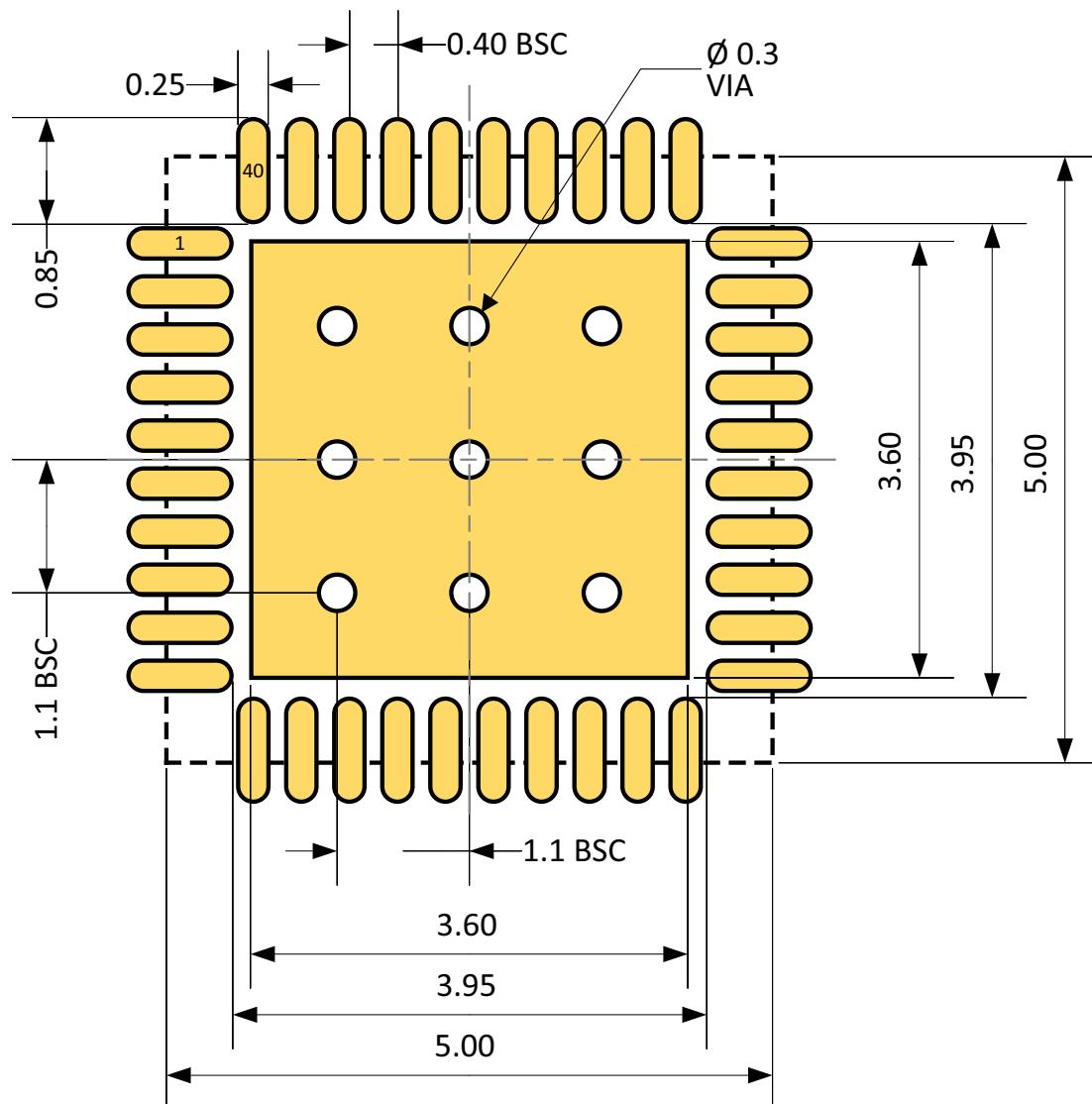


Figure 22: Recommended board layout for QFN40 package (all dimensions in mm)



15. Glossary

15.1. SRCx Acronyms

V_{SRCx}

Voltage on the $SRCx$ pin.

$V_{SRCx,CS}$

Minimum voltage required on $SRCx$ for the AEM13920 to coldstart.

$V_{SRCx,REG}$

Target regulation voltage of the source, depending on $SRCx_CFG[4:0]$ configuration or I²C register (when $SRCx$ regulation mode is constant voltage).

V_{MPP}

Target regulation voltage on $SRCx$ when extracting power (when $SRCx$ regulation mode is MPPT).

V_{OC}

Open circuit voltage of the harvester connected on $SRCx$.

V_{SRCLOW}

V_{SRCx} threshold below which the AEM13920 switches to **SLEEP STATE**, as described in Section 9.10.

C_{SRCx}

Decoupling capacitor on $BUFSRCx$ pin.

I_{SRCx}

Current extracted from the harvester connected on $SRCx$.

L_{BOOSTx}

Boost converter x inductor.

R_{MPPT}

For the boost converters, ratio between the open circuit voltage V_{OC} and the voltage regulation V_{MPP} determined by the MPPT (when the boost converter is in MPPT mode).

$I_{LBOOST,PEAK}$

Peak current in L_{BOOSTx} when the boost converter is running.

$T_{MPPT,PERIOD}$

Time between two MPP evaluations (see Table 12).

$T_{MPPT,SAMPLING}$

Open-circuit duration for the MPP evaluations (see Table 12).

R_{ZMPP}

Resistor used for ZMPP module, connected between $SRC1$ and $ZMPP$.

15.2. STO Acronyms

V_{STO}

Voltage on the STO pin.

V_{OVDIS}

Minimum voltage accepted on the storage element before stopping to supply **LOAD** (see Section 6.4).

V_{CHRDY}

Minimum voltage accepted on the storage element before starting to supply **LOAD** in **START STATE** (see Section 6.4).

V_{OVCH}

Maximum voltage accepted on the storage element before disabling its charging (see Section 6.4).

C_{STO}

Decoupling capacitor on STO pin.

I_{QSHIP}

Quiescent current drawn on the storage element when the AEM13920 is in shipping mode ($SHIP_MODE$ is HIGH) and that no energy is available on $SRCx$ (the AEM13920 is off in that case).

$I_{QSHIP,SRCx}$

Current drawn on the storage element when the AEM13920 is in shipping mode and energy is available on $SRCx$.

I_{QOFF}

Current drawn on the storage element when the AEM13920 is in **RESET STATE**.

15.3. VINT Acronyms

V_{INT}

Voltage on the $VINT$ pin.

$V_{INT,CS}$

Minimum voltage on $VINT$ to allow the AEM13920 to switch from **RESET STATE** to **SENSE STO STATE**.

$V_{INT,RESET}$

Minimum voltage on $VINT$ before switching to **RESET STATE** (from any other state).

C_{INT}

Decoupling capacitor on $VINT$ pin.



I_{QSLEEP}

Quiescent current drawn on **STO** when the AEM13920 is in **SLEEP STATE**.

I_{QSUPPLY}

Quiescent current drawn on **STO** when the AEM13920 is in **SUPPLY STATE**.

15.4. I²C Acronyms

V_{VDDIO}

Voltage on the **VDDIO** pin.

R_{SCL} / R_{SDA}

Pull-up resistors used for the I²C communication bus.

15.5. LOAD Acronyms

V_{LOAD}

Voltage on the **LOAD** pin.

C_{LOAD}

Decoupling capacitor on **LOAD** pin.

L_{BUCK}

Buck converter inductor.

I_{BUCK,PEAK}

Peak current in **L_{BUCK}** when the buck converter is running.

15.6. 5V_IN Acronyms

V_{5V_IN}

Voltage on **5V_IN** pin.

V_{5V_IN,MIN}

Minimum voltage on **5V_IN** pin.

C_{5V}

Decoupling capacitor on **5V_IN** pin.

I_{5V,CC}

Current provided to the storage element by the **5V_IN** when in constant current mode.

I_{5V,CV}

Current provided to the storage element by the **5V_IN** when in constant voltage mode.

R_{5V_IMAX}

Resistor connected between **5V_IMAX** and **GND** that defines the maximum current provided to the storage element by the 5 V charger (**5V_IN** pin).

T_{5V,RISE}

Minimum voltage rise time on the **5V_IN** pin.

R_{5V} / C_{5V}

Respectively, resistor and capacitor creating a RC filter on **5V_IN** to limit **T_{5V,RISE}**.

D_{5V}

Zener diode that ensures that the voltage on **5V_IN** stays below 5.5 V at any time.

P_{R5V,idle}

Power dissipated by **R_{5V}** when no current is pulled by the 5 V charger (current only flowing in the zener protection diode).

P_{R5V,CC}

Power dissipated by the **R_{5V}** when the 5 V charger is in constant current (CC) mode.

15.7. Various Acronyms

R_{TH}

Along with **R_{DIV}**, thermistor creating a resistive voltage divider connected to **TH_MON**, used for thermal monitoring.

R_{DIV}

Along with **R_{TH}**, resistor creating a resistive voltage divider connected to **TH_MON**, used for thermal monitoring.

T_{CRIT}

In **SUPPLY STATE**, the AEM13920 waits for **T_{CRIT}** before switching to **OVDIS STATE** when **V_{STO}** drops below **V_{OVDIS}**.

T_{GPIO,MON}

GPIO reading rate.

T_{MULT}

Boost or buck converter inductor charging timing multiplier.

T_{TEMP,MON}

Temperature monitoring rate.



16. Revision History

Revision	Date	Description
1.0	April, 2023	Creation of the document.
1.1	August, 2023	<p>Finished register descriptions.</p> <p>Added:</p> <ul style="list-style-type: none">- I²C protocol.- Efficiencies.- Behavior graphs.- Typical application circuits.- Glossary.- Quiescent currents.
1.2	September, 2023	<p>Added:</p> <ul style="list-style-type: none">- Missing storage element voltage info on buck efficiency graph.- Boost efficiency graph: source current as graph title instead of x axis title.- Minimum BOM section.- Updated minimum cold-start power.
1.3	December, 2023	<ul style="list-style-type: none">- Replaced "0/1" by "L/H" for configuration pins.
1.4	April, 2024	<ul style="list-style-type: none">- Layout improvements.- Added precision about CTRL and IRQFLGx registers.- Fixed RDIV part number in "Minimum BOM" table.- Added PCB routing/layout guidelines.- Minimum BOM table: LBUCK unit "μH" instead of "μF".- Boost efficiency: source voltage noted "VSRC" instead of "VMPP".- Reordered register descriptions to regroup them by functionality.- Added cautionary statement for storage element threshold voltages.- Added C5V decoupling capacitor.- Fixed typo in I2C protocol description figure.
1.5	June, 2024	<ul style="list-style-type: none">- BSTxCFG register configuration: added recommended inductor values.- Added cautionary statement along with storage element threshold voltages.- Added CSTO min. and typical value in "Recommended external components" table.- Behavior section: fixed typo in SRC1 configuration (VOVCH changed to VOC).

Table 67: Revision history (part 1)



Revision	Date	Description
1.6	November, 2024	<ul style="list-style-type: none">- Fixed EVK part number on first page.- Updated application list on first page.- Updated minimum source regulation voltage to 0.120 V.- Renamed “Performance Data” section to “Typical Characteristics”.- Created a “Specifications” section to place the characteristic and ratings sections in it.- Added operating temperature, storage temperature, and minimum input voltage values in “Absolute Maximum Ratings”.- Added ESD ratings and thermal resistance θ_{JA} and θ_{JC} values.- In “Electrical Characteristics” table:<ul style="list-style-type: none">- Updated V_{MPP} and $V_{SRCx,REG}$ maximum values.- Added I_{QOFF}.- Updated the quiescent currents.- Corrected $T_{MPPT,PERIOD}$ minimum and maximum values.- Added precisions about optional/mandatory components in “Recommended external components” table.- Added precisions about C_{SRCx} value range.- Updated minimum L_{BOOSTx} and L_{BUCK} values according to boost/buck timings.- Updated L_{BUCK} typical value to 10 μH in the “Recommended external components” table.- Aesthetic modifications on “AEM13920 state machine” figure.- Explained 5V_IN voltage minimum rise time and minimum value.- Added R5V resistor in figures, typical application circuits and 5 V charger sections.- Renamed “Source Voltage Regulation” sections to “Source Constant Voltage Regulation”.- Added “Boost Converter Timings” and “Buck Converter Timings” sections in “System Configuration” to specify the timings default values.- Added explanation detailing that the I²C interface will be disabled if I²C pins are read LOW during SENSE STO STATE.- Fixed rounding errors on SRCx related voltages.- Rounded all source regulation voltages to 3 decimal places.- Renamed “sleep threshold” to “source low threshold” for disambiguation.- Changed “I²C Serial Interface Protocol”, “Register Map” and “Registers Configuration” subsections to sections.- Corrected CTRL.SYNCBUSY bit to read only “R” instead of read and write in the “Register map” table.- SRCxREGUx.LVL register: lowest source regulation voltages lead to SRCx being considered as “source low”.- SRCx register: fixed formula ranges as well as lookup table ranges.- Removed the ambiguous “interrupt” term about the IRQ pin.- Modified L_{BOOST1} to 15 μH instead of 10 μH in “Typical application circuit 2”.- Added calculations for R5V, C5V and D5V to example circuits 1 and 3 sections.- Added Moisture Sensitivity Level, RoHS Compliance and REACH Compliance in “Package Information” section.- Updated package dimensions and added markings in “QFN 40-pin 5x5mm drawing” figure.- Updated board layout dimensions and added vias in “Recommended board layout for QFN40 package” figure.
1.7	December, 2024	Fixed various typos throughout the document.

Table 67: Revision history (part 2)