Highly Efficient, Regulated Dual-Output, Ambient Energy Manager for Source Voltage Level Configuration with Optional Primary Battery

Features

Ultra-low power start-up

- Cold start from 380 mV input voltage and 3 µW input power (typical).

Constant input voltage regulation

- Optimized for constant voltage PV cells, intermittent and pulsed power.
- Input voltage range from 50 mV to 5 V.
- Selectable operating input voltage regulation from 50 mV to 4.5 V.
- Up to 110 mA current extracted from the harvester.

Integrated 1.2 V/1.8 V LDO regulator

- Up to 20 mA load current.
- Dynamically power-gated by external control.
- Selectable output voltage.

Integrated 1.8 V - 4.1 V LDO regulator

- Up to 80 mA load current with 300 mV drop-out.
- Dynamically power-gated by external control.
- Selectable or adjustable output voltage.

Flexible energy storage management

- Selectable or adjustable overcharge and over-discharge protection for any type of rechargeable battery or (super)capacitor.
- Fast supercapacitor charging.
- Indication when battery is running low.
- Indication when output voltage regulators are available.

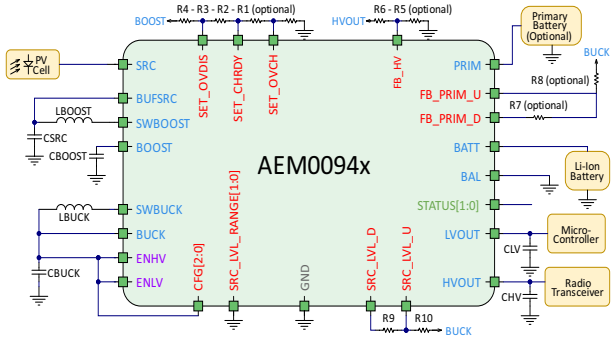
Optional primary battery

- Automatic switching to primary battery when the secondary battery is exhausted.

Integrated storage element balancing circuit for dual-cell supercapacitor

Applications

Door access systems	Smart wearable sensors
Smart switches home/building	Point-of-Sales (POS)



Description

The AEM0094x is an integrated energy management circuit that extracts DC power to simultaneously store energy in a rechargeable element and supply the system with two independent regulated voltages. The AEM0094x allows to extend battery lifetime and ultimately eliminate the primary energy storage element in a large range of sources such as constant voltage PV cells, pulsed sources, intermittent sources, capacitive sources and constant MPP sources.

The AEM0094x harvests the available input current up to 110 mA while regulating the source to a voltage configured by the user. It integrates an ultra-low power boost converter to charge a storage element, such as a Li-ion battery, a thin film battery, a supercapacitor or a conventional capacitor.

The input regulation voltage at which the AEM operates can be set within the 50 mV to 4.5 V range thanks to a resistive divider. With its unique cold-start circuit, it can start operating with empty storage elements at an input voltage as low as 380 mV and an input power of only 3 µW.

The low-voltage supply typically drives a microcontroller at 1.2 V or 1.8 V. The high-voltage supply typically drives a radio transceiver at a configurable voltage between 1.8 V and 4.1 V. Both are driven by highly-efficient LDO (Low Drop-Out) linear regulators for low noise and high stability.

Configuration pins determine various operating modes by setting predefined conditions for the energy storage element (overcharge or overdischarge voltages), and by selecting the voltage of the high-voltage supply and the low-voltage supply.

The chip integrates all active elements for powering a typical wireless sensor. Five capacitors, two inductors and two resistors are required, all available in small packages. With only nine external components, integration is maximized, footprint and BOM are minimized, optimizing the time-to-market and the costs of designs.

The AEM00941 allows higher efficiencies using a larger inductor value (typ. 100 µH), while the AEM00940 allows smaller PCB size using a smaller inductor value (typ. 10 µH or 22 µH).

Device Information

Part Number	Package	Body Size
10AEM00940C0000	QFN 28-pin	5x5mm
10AEM00941C0000	QFN 28-pin	4x4mm

Evaluation Board

AEM0094x evaluation boards are available at *e-peas.com*.

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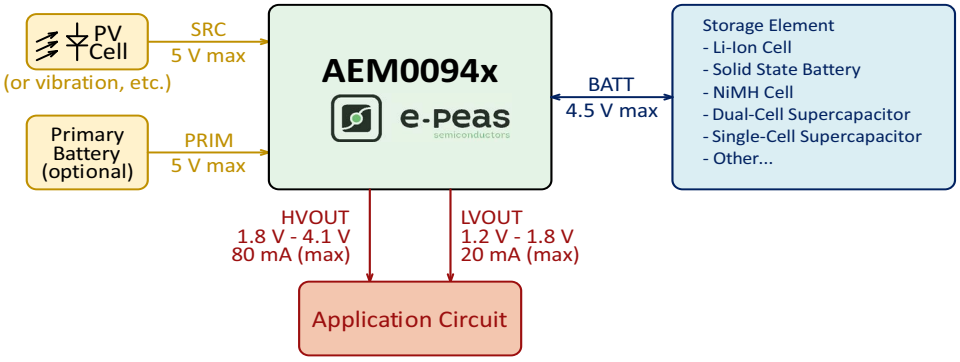

Figure 1: Simplified schematic view

1. Introduction

The AEM0094x is a full-featured energy efficient power management circuit capable of charging a storage element (battery or supercapacitor, connected to BATT) from an energy source (connected to SRC) as well as supplying loads at different operating voltages through two power supplying LDO regulators (LVOUT and HVOUT).

The heart of the AEM0094x is a cascade of two regulated switching converters, namely the boost converter and the buck converter, both with high power conversion efficiencies (See Section 12).

At first start-up, as soon as a required cold-start voltage of 380 mV and a scant amount of power of only 3 µW are available from the harvested energy source, the AEM coldstarts. After the cold start, the AEM can extract the power available from the source and regulate the source at the voltage configured by the user.

Through three configuration pins (CFG[2:0]), the user can select a specific operating mode from a range of seven modes that covers most application requirements without any dedicated external component. These operating modes define the LDO output voltages and the protection levels of the storage element. A custom mode allows the user to define arbitrary storage element protection levels and the output voltage of the high-voltage LDO (See Section 9.1).

The source regulation voltage $V_{SRC,REG}$ can be adapted to the harvester thanks to two resistors and two configuration pins (SRC_LVL_RANGE[1:0]).

Two logic control pins (ENLV and ENHV) allow to dynamically activate or deactivate the LDO regulators that supply the low and high voltage load. The status pin STATUS[0] alerts the user that the LDOs are operational and can be enabled. This signal can also be used to enable an optional external regulator.

If the battery voltage gets depleted, LVOUT and HVOUT are power-gated and the controller is no longer supplied by the storage element to protect it from further discharge. Around 600 ms before the shutdown of the AEM, the status pin STATUS[1] alerts the user for a clean shutdown of the system.

However, if the storage element gets depleted and an optional primary battery is connected on PRIM, the AEM0094x automatically uses it as a source to recharge the storage element before switching back to the ambient source. This guarantees continuous operation even under the most adverse conditions (See Section 8.2.4). STATUS[1] is asserted when the primary battery is providing power.

2. Pin Configuration and Functions

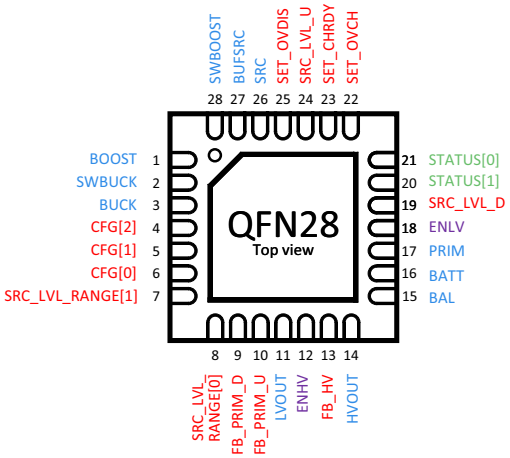

Figure 2: Pinout diagram QFN 28-pin

Name	Pin Number	Function
Power pins		
BOOST	1	Output of the boost converter.
SWBUCK	2	Switching node of the buck converter.
BUCK	3	Output of the buck converter.
LVOUT	11	Output of the low voltage LDO regulator.
HVOUT	14	Output of the high voltage LDO regulator.
BAL	15	Connection to the mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.
BATT	16	Connection to the energy storage element, battery or capacitor. Cannot be left floating.
PRIM	17	Connection to the primary battery (optional). Must be connected to GND if not used.
SRC	26	Connection to the harvested energy source.
BUFSRC	27	Connection to an external capacitor buffering the boost converter input.
SWBOOST	28	Switching node of the boost converter.
Configuration pins		
CFG[2]	4	Used for the configuration of the threshold voltages of the energy storage element and the output voltage of the LDOs.
CFG[1]	5	
CFG[0]	6	
SRC_LVL_RANGE[1]	7	Used for the configuration of the range for the source voltage regulation (see Section 9.2). Cannot be left floating.
SRC_LVL_RANGE[0]	8	
SRC_LVL_D	19	Used for the configuration of the source voltage regulation. Cannot be left floating.
SRC_LVL_U	24	
FB_PRIM_D	9	Used for the configuration of the primary battery overdischarge voltage (optional). Must be connected to GND if not used.
FB_PRIM_U	10	
FB_HV	13	Used for the configuration of the high-voltage LDO when in custom mode (optional). Must be left floating if not used.
SET_OVCH	22	Used for the configuration of the threshold voltages for the energy storage element when in custom mode (optional). Must be connected to BUCK if not used.
SET_CHRDY	23	
SET_OVDIS	25	

Table 1: Pins description (Part 1)

Name	Pin Number	Function
Control pins		
ENHV	12	Enabling pin for the high-voltage LDO (See Table 7).
ENLV	18	Enabling pin for the low-voltage LDO (See Table 7).
Status pins		
STATUS[1]	20	Logic output. Asserted during 600 ms if the battery voltage falls below V_{OVDIS} or asserted as long as the AEM is taking energy from the primary battery.
STATUS[0]	21	Logic output. Asserted when the LDOs can be enabled.
Other pins		
GND	Exposed pad	Ground connection, should be solidly tied to the PCB ground plane.

Table 1: Pins description (Part 2)

3. Absolute Maximum Ratings

Parameter	Rating
Voltage on SRC, BUFSRC, BATT, BAL, PRIM, BOOST, SWBOOST, HVOUT, ENLV	5.5 V
Voltage on BUCK, SWBUCK, LVOUT, CFG[2:0], FB_PRIM_U, FB_PRIM_D, SRC_LVL_RANGE[1:0], SRC_LVL_U, SRC_LVL_D, SET_OVDIS, SET_CHRDY, SET_OVCH, ENHV	2.75 V
Voltage on FB_HV	2.5 V
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Table 2: Absolute maximum ratings

4. Thermal Resistance

Package	θJA	θJC	Unit
QFN 28-pin	38.3	2.183	°C/W

Table 3: Thermal data

ESD CAUTION		
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality	
VESD	Human-body model according to Jedec JS001-2017	± 500 V
	Charge device model according to Jedec JS002-2014	± 1000 V

Table 4: ESD caution

5. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input voltage and input power						
P_{SRC_CS}	Source power required to coldstart.	During cold start.	3			µW
V_{SRC}	Input voltage of the energy source (maximum given by the open-circuit voltage).	During cold start.	0.38		5	V
		After cold start.	0.05[1]		5	
V_{SRC_REG}	Regulation voltage of the source.		0.05		4.5	V
I_{SRC}	Harvested current from the energy source.	AEM00940: L_{BOOST} = 10 µH			110	mA
		AEM00940: L_{BOOST} = 22 µH			50	
		AEM00941: L_{BOOST} = 100 µH			10	
DC-DC converters						
V_{BOOST}	Output voltage of the boost converter.	During normal operation.	2.2		4.5	V
V_{BUCK}	Output voltage of the buck converter.		2	2.2	2.5	
I_{BUCK}	Total load current supplied by the BUCK converter (including LVOUT current I_{LV}).	L_{BUCK} = 10 µH.	0		20	mA
		L_{BUCK} = 4 µH.	0		50	mA
Storage element						
V_{BATT}	Voltage on the storage element.		0[2]		4.5	V
V_{PRIM}	Voltage on the primary battery.		0.6		4.5	V
I_{PRIM}	Current from the primary battery.			20		mA
$V_{FB\_PRIM\_U}$	Feedback for defining the overdischarge voltage level on the primary battery.		0.15		1.1	V
$V_{SRC\_LVL\_U}$	Source feedback voltage on SRC_LVL_U pin.		0		1.35	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling the boost converter.	See Table 8.	2.3		4.5	V
V_{CHRDY}	Minimum voltage required on the storage element before enabling the LDO when coming from WAKE-UP MODE.	After cold start See Table 8.	2.25		4.45	V
V_{OVDIS}	Minimum voltage accepted on the storage element before switching to primary battery or entering SHUTDOWN MODE.	See Table 8.	2.2		4.4	V
I_Q	Quiescent current on BATT when the boost converter is not running.	V_{BATT} = 3 V; LDOs disabled.		400		nA
		V_{BATT} = 3 V; LDOs enabled.		600		nA
Low-Voltage LDO regulator						
V_{LV}[3]	Output voltage of the low-voltage LDO.	See Table 8.	1.2		1.8	V
I_{LV}	Load current supplied by the low-voltage LDO.	L_{BUCK} = 10 µH.	0		20	mA
High-Voltage LDO regulator						
V_{HV}[4]	Output voltage of the high-voltage LDO.	See Table 8.	1.8		V_{OVDIS} - 0.3 V	V
I_{HV}	Load current supplied by the high-voltage LDO.		0		80	mA

Table 5: Electrical characteristics (Part 1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Timing						
$T_{VSRC\_REG,UPDATE}$	Time between two updates of the source voltage regulation (see Section 8.3).			20		s
T_{CRIT}	Time before shutdown once STATUS[1] has been asserted (see Section 8.2.5 and Figure 5).		400	600	800	ms
Logic output pins						
STATUS[1:0]	Logic output levels on the status pins.	Logic HIGH (H).	V_{BATT} - 0.1	V_{BATT}	V_{BATT} + 0.1	V
		Logic LOW (L).	GND - 0.1	GND	GND + 0.1	V

Table 5: Electrical characteristics (Part 2)

1. Minimum V_{SRC} value for harvesting capabilities after coldstart.
2. To stay in NORMAL MODE, V_{BATT} minimum voltage must stay above V_{OVDIS}.
3. The variability of V_{LV} at 1 mA is 1% (typical and preliminary result from simulations).
4. The variability of V_{HV} at 1 mA is 1.3% (typical and preliminary result from simulations).

6. Recommended Operation Conditions

Symbol	Parameter		Min	Typ	Max	Unit
External components						
C_{SRC}	BUFSRC pin decoupling capacitor.		8	10	22	µF
C_{BOOST}	Output capacitor of the boost converter.		10	22		µF
L_{BOOST}	Inductor of the boost converter.	AEM00940	4	10		µH
		AEM00941		100		µH
C_{BUCK}	Output capacitor of the buck converter.		8	10		µF
L_{BUCK}	Inductor of the buck converter.		4	10	25	µH
C_{LV}	Low-voltage LDO regulator decoupling capacitor.		8	10	14	µF
C_{HV}	High-voltage LDO regulator decoupling capacitor.		8	10	14	µF
C_{BATT}	Optional - Capacitor connected on BATT if no storage element is connected (see Section 9.4 and Section 9.6).	LDOs disabled.	22			µF
		LDOs enabled.	150			µF
R_T	Optional - Sum of resistors for setting battery protection threshold voltages in custom mode. R_T = R1 + R2 + R3 + R4 (see Section 9.1).		1	10	100	MΩ
R_V	Optional - Sum of resistors for setting the output voltage of the high-voltage LDO in custom mode. R_V = R5 + R6 (see Section 9.1).		1	10	40	MΩ
R_P	Optional - Sum of resistors used to define the primary battery minimum voltage. R_P = R7 + R8 (see Section 9.3).		100		500	kΩ
R_S	Sum of resistors used to define the source voltage regulation. R_S = R9 + R10 (see Section 9.2).		0.1		1	MΩ
Logic input pins						
ENHV	Enabling pin for the high-voltage LDO.	Logic HIGH (H).	Connect to BUCK.			
		Logic LOW (L).	Connect to GND.			
ENLV	Enabling pin for the low-voltage LDO.	Logic HIGH (H).	Connect to BUCK or BOOST.			
		Logic LOW (L).	Connect to GND.			
CFG[2:0]	Configuration pins for the storage element protection threshold voltages (see Table 8).	Logic HIGH (H).	Connect to BUCK.			
		Logic LOW (L).	Connect to GND.			
SRC_LVL_RANGE[1:0]	Configuration pins for the source voltage regulation range.	Logic HIGH (H).	Connect to BUCK.			
		Logic LOW (L).	Connect to GND.			

Table 6: Recommended operating conditions

7. Functional Block Diagram

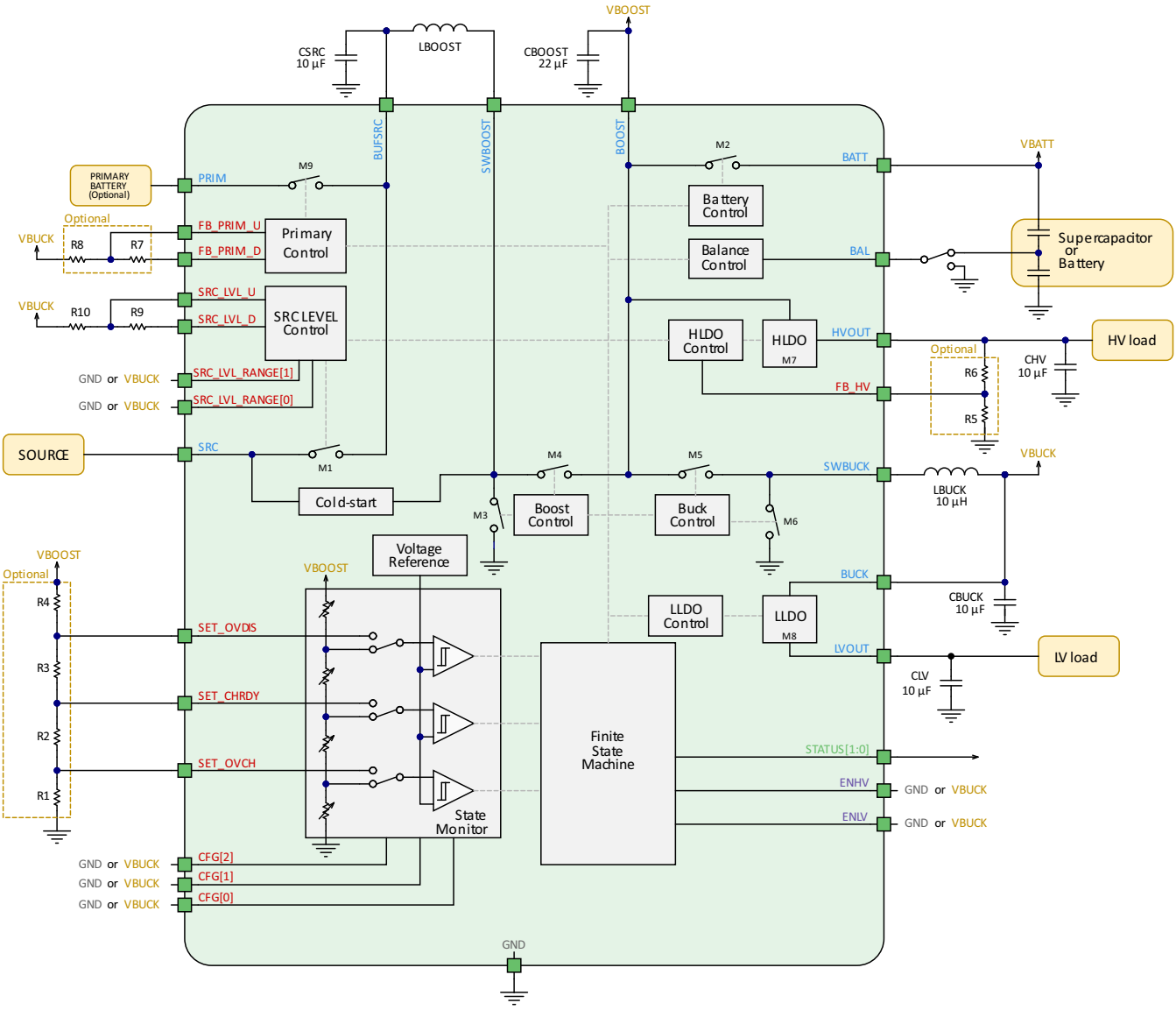

Figure 3: Functional block diagram

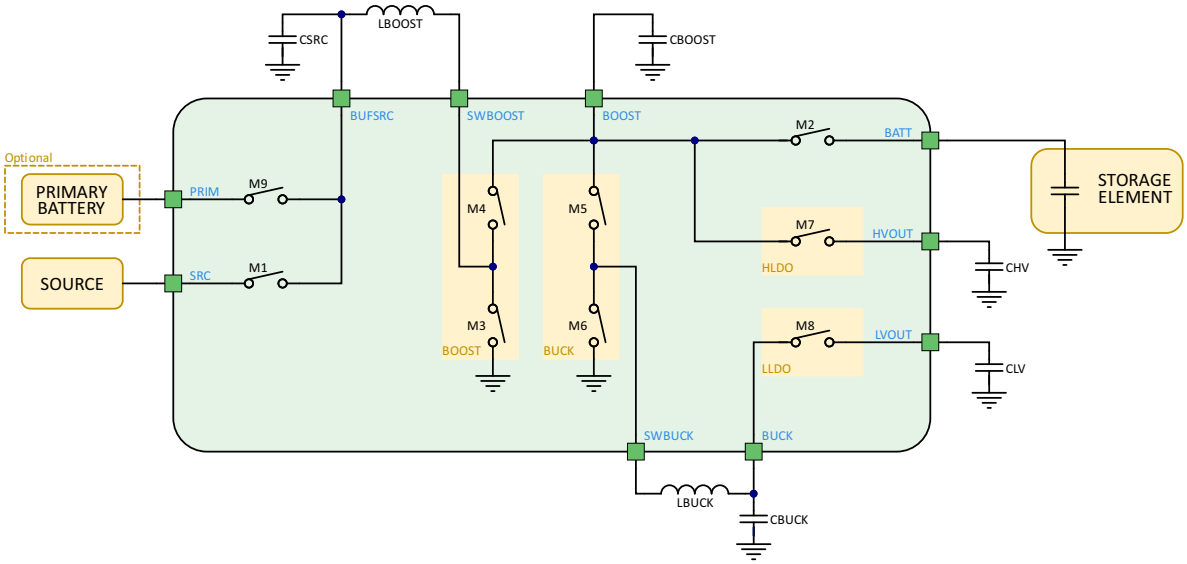

Figure 4: Simplified schematic view of the AEM0094x

8. Theory of Operation

8.1. Power Converters

8.1.1. Boost Converter

The boost (or step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.2 V to 4.5 V, according to the system configuration. This voltage (V_{BOOST}) is available at the BOOST pin.

The switching transistors of the boost converter are M3 and M4, with the switching node available externally at SWBOOST. The reactive power components of this converter are the external inductor L_{BOOST} and the external capacitor C_{BOOST}.

The regulation control circuit periodically disconnects the source from BUFSRC pin with the transistor M1 in order to measure the voltage present on SRC_LVL_U and define the source regulation voltage.

BUFSRC is decoupled by the capacitor C_{SRC}, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the BATT pin. Its voltage is named V_{BATT}. This node is linked to BOOST through the transistor M2. In NORMAL MODE (see Section 8.2.2), this transistor effectively shorts the battery to the BOOST node (V_{BATT} = V_{BOOST}). When energy harvesting is occurring, the boost converter delivers a current that is shared between the battery and the LDOs. M2 is opened to disconnect the storage element when V_{BATT} reaches V_{OVDIS}. However, in such a scenario, the AEM0094x offers the possibility of connecting a primary battery to recharge V_{BATT} up to V_{CHRDY}. The transistor M9 connects PRIM to BUFSRC and the transistor M1 is opened to disconnect the SRC input pin as explained in the PRIMARY BATTERY MODE section.

More explanations about the different modes can be found in Section 8.2.

8.1.2. Buck Converter

The buck (or step-down) converter lowers the voltage from V_{BOOST} to a constant V_{BUCK} value of 2.2 V. This voltage is available at the BUCK pin. The switching transistors of the buck converter are M5 and M6, with the switching node available externally at SWBUCK. The reactive power components of the buck converter are the external inductor L_{BUCK} and the external capacitor C_{BUCK}.

8.1.3. LDO Outputs

Two Low Drop-Out linear regulators are available to supply loads at different operating voltages:

- Through M7, BOOST supplies the high-voltage LDO that powers its load through HVOUT. This regulator delivers a clean voltage named V_{HV}. When using the built-in configuration modes, an output voltage of 1.8 V, 2.5 V or 3.3 V can be selected. When using the custom configuration mode, V_{HV} is adjustable between 1.8 V and V_{OVDIS} - 0.3 V. The output is decoupled by the external capacitor C_{HV}.
- Through M8, V_{BUCK} supplies the low-voltage LDO that powers its load through LVOUT. This regulator delivers a clean voltage named V_{LV} of 1.2 V or 1.8 V. The output is decoupled by the external capacitor C_{LV}.

See Table 5 for HVOUT and LVOUT maximum current values (respectively I_{HV} and I_{LV}).

Both the high-voltage and the low-voltage outputs can be dynamically enabled or disabled respectively with the logic control pins ENHV and ENLV (see Table below).

ENLV	LVOUT
L	Disabled
H	Enabled

ENHV	HVOUT
L	Disabled
H	Enabled

Table 7: LDOs configurations

8.2. Operating Modes

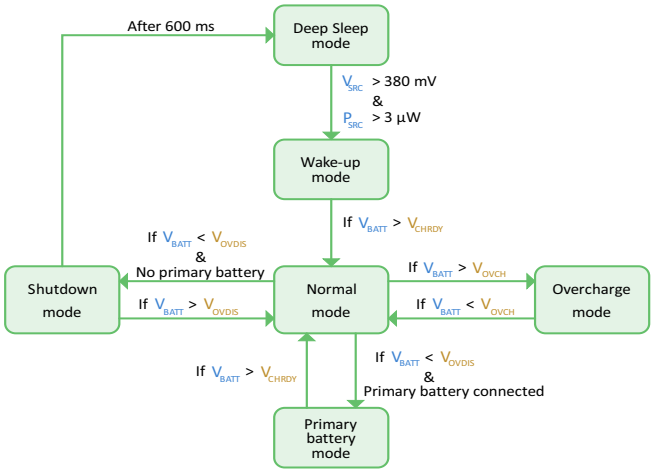

Figure 5: Diagram of the AEM0094x modes

8.2.1. Deep Sleep & Wake Up Modes

The DEEP SLEEP MODE is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold-start voltage of 380 mV and the required power of 3 µW becomes available on SRC, the WAKE-UP MODE is activated. V_{BOOST} and V_{BUCK} rise up to a voltage of 2.2 V. V_{BOOST} then rises up to V_{OVCH}.

At this stage, both LDOs are internally disabled. Therefore, STATUS[0] is low as shown in Figure 11 and Figure 12.

When V_{BOOST} reaches V_{OVCH}, two scenarios are possible:

- In the first scenario, a supercapacitor or a capacitor having a voltage lower than V_{CHRDY} is connected to the BATT node (see Section 8.2.1.1).
- In the second scenario, a charged battery is connected to the BATT node (see Section 8.2.1.2).

8.2.1.1. Supercapacitor as a Storage Element

If the storage element is a supercapacitor, the storage element may need to be charged from 0 V. The boost converter charges BATT from the input source and by modulating the conductance of M1 and M2. During the charge of the BATT node, both LDOs are disabled and STATUS[0] is set to low. When V_{BATT} reaches V_{CHRDY}, the circuit enters NORMAL MODE, STATUS[0] is asserted and the LDOs can be enabled by the user using ENLV and ENHV control pins as shown in Figure 11.

8.2.1.2. Battery as a Storage Element

If the storage element is a battery but its voltage is lower than V_{CHRDY}, the storage element first needs to be charged until it reaches V_{CHRDY}. This allows a safety margin to ensure that the storage element is able to provide the required power before enabling the outputs (LDOs).

Once V_{BATT} exceeds V_{CHRDY}, or if the battery was initially charged above V_{CHRDY}, the circuit enters NORMAL MODE. STATUS[0] is asserted and the LDOs can be dynamically enabled or disabled through ENLV and ENHV as shown in Figure 12.

8.2.2. Normal Mode

Once the AEM enters NORMAL MODE, it stays in this mode as long as the following condition is met:

$$V_{OVDIS} < V_{BATT} < V_{OVCH}$$

The AEM0094x will switch to another mode in the following cases:

- V_{BATT} increases above V_{OVCH} because the source provides more power than the load consumes. The circuit enters OVERCHARGE MODE, as explained in Section 8.2.3.
- V_{BATT} falls below V_{OVDIS} due to a lack of power from the source. In this case, either the circuit enters SHUTDOWN MODE as explained in Section 8.2.5, or, if a charged primary battery is connected on PRIM, the circuit enters PRIMARY BATTERY MODE as explained in Section 8.2.4.

8.2.3. Overcharge Mode

When V_{BATT} reaches V_{OVCH}, the battery charge is complete. The AEM maintains V_{BATT} around V_{OVCH}, with a hysteresis of a few mV as shown in Figure 13, to prevent damage to the storage element and to the internal circuitry. In this configuration, the boost converter is periodically activated to maintain V_{BATT} and the LDOs are available. Moreover, when the boost converter is not activated, the transistor M1 in Figure 4 is opened to prevent current from the source to the storage element when V_{SRC} is higher than V_{OVCH}.

8.2.4. Primary Battery Mode

When V_{BATT} drops below V_{OVDIS}, the circuit compares the voltage on PRIM with the voltage on FB_PRIM_U to determine whether a charged primary battery is connected on PRIM. The voltage on FB_PRIM_U is set thanks to two optional resistors as explained in Section 9.3.

If the following formula is true, the circuit considers the primary battery as available and the circuit enters PRIMARY BATTERY MODE.

$$\frac{V_{PRIM}}{4} > V_{FB\_PRIM\_U}$$

In that mode, transistor M1 is opened and the primary battery is connected to BUFSRC through transistor M9 to become the source of energy of the AEM0094x. STATUS[1] is asserted as long as the chip is in PRIMARY BATTERY MODE.

The AEM remains in this mode until V_{BATT} reaches V_{CHRDY}. At that point, the circuit enters NORMAL MODE.

If no primary battery is used in the application, PRIM, FB_PRIM_U and FB_PRIM_D must be tied to GND.

8.2.5. Shutdown Mode

When V_{BATT} drops below V_{OVDIS} and no power is available from a primary battery, the circuit enters SHUTDOWN MODE, as shown in Figure 14, to prevent deep discharge that could damage the storage element and make the LDOs unstable. The circuit asserts STATUS[1] to warn the application that a shutdown may occur. Both LDO regulators remain enabled during the next 600 ms (T_{CRIT}).

If no primary battery is used, this mechanism allows the application circuit, whether it is powered on LVOUT or HVOUT, to trigger an interrupt by the low to-high transition of STATUS[1], and to take all appropriate actions before LVOUT and HVOUT are disabled.

If V_{BATT} recovers to V_{OVDIS} within T_{CRIT} (about 600 ms), the AEM switches back to NORMAL MODE. But if, after T_{CRIT}, V_{BATT} does not reach V_{OVDIS}, the circuit enters DEEP SLEEP MODE. Both LDOs are disabled and BATT is disconnected from BOOST to avoid damaging the battery due to the overdischarge. From now on, the AEM must go through the wake-up procedure described in the Section 8.2.1.

8.3. Source Voltage Regulation

During NORMAL MODE, SHUTDOWN MODE and a part of WAKE-UP MODE, the source voltage (V_{SRC_REG}) is regulated thanks to the evaluation of the voltage on the SRC_LVL_U pin and the gain set by SRC_LVL_RANGE[1:0] pins:

$$V_{SRC\_REG} = V_{SRC\_LVL\_U} \cdot \text{Gain}$$

With the resistive divider shown in Figure 7, the AEM0094x measures $V_{SRC\_LVL\_U}$ by connecting SRC_LVL_D to GND internally. This evaluation is performed every $T_{VSRC\_REG,UPDATE}$ (20 s).

$V_{SRC\_LVL\_U}$ is then multiplied by the gain to define the source voltage regulation. Three different gain values are available through the configuration pins SRC_LVL_RANGE[1:0] as shown in Table 9.

With the exception of this evaluation process, the source voltage V_{SRC} is continuously compared to V_{SRC_REG}:

- When V_{SRC} exceeds V_{SRC_REG} by a small hysteresis, the boost converter is switched on, extracting electric charges from the source, thus lowering its voltage.
- When V_{SRC} falls below V_{SRC_REG} by a small hysteresis, the boost converter is switched off, allowing the harvester to accumulate new electric charges into C_{SRC}, which voltage rises.

8.4. Storage Element Balancing Circuit for Dual-cell Supercapacitor

When using a dual-cell supercapacitor, it is necessary to keep both cells at similar voltages to avoid damage due to a potential over-voltage on one cell. This is ensured by the AEM0094x storage element balancing circuit.

If a battery, a capacitor or a single-cell supercapacitor is connected on BATT, BAL is connected to GND and the storage element balancing circuit is disabled.

If a dual-cell supercapacitor is connected on BATT, BAL is connected to the node between the two cells of the supercapacitor. The storage element balancing circuit compensates for any mismatch of the two cells that could overcharge one of both cells. It ensures that BAL remains close to V_{BATT} / 2.

9. System Configuration

9.1. Battery and LDOs Configuration

Configurations pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell supercapacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode - Programmable through R1 to R6.				1.8 V	

Table 8: Usage of CFG[2:0]

Through three configuration pins (CFG[2:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 8. The three threshold levels are defined as:

- V_{OVCH}: maximum voltage accepted on the storage element before disabling the boost converter.
- V_{CHRDY}: minimum voltage required on the storage element after a cold start before enabling the LDOs.
- V_{OVDIS}: minimum voltage accepted on the storage element before considering the storage element as depleted.

See Section 8 for more information about the purposes of these thresholds.

The two LDOs output voltages are called V_{HV} and V_{LV} for the high and low output voltages respectively. Seven combinations of these voltage levels are hard-wired and selectable through the CFG[2:0] configuration pins, covering most application cases. For other V_{OVCH}, V_{CHRDY}, V_{OVDIS} and V_{HV} voltages combinations, a custom mode is available. In this mode, the user can define those voltages with resistors, connected to the pins named SET_OVDIS, SET_CHRDY, SET_OVCH and FB_HV.

When the custom mode is not used, SET_OVDIS, SET_CHRDY and SET_OVCH pins must be connected to V_{BUCK} and FB_HV must be left floating.

9.1.1. Custom Mode

When CFG[2:0] are tied to GND, the custom mode is selected. All six resistors, shown in Figure 6, are used to configure the custom mode as follows:

V_{OVCH}, V_{CHRDY} and V_{OVDIS} are defined thanks to R1, R2, R3 and R4. The resistors are calculated as follows:

- $R_T = R1 + R2 + R3 + R4$
- $1M\Omega \leq R_T \leq 100M\Omega$
- $R1 = R_T \cdot \frac{1V}{V_{OVCH}}$
- $R2 = R_T \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}}\right)$
- $R3 = R_T \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}}\right)$
- $R4 = R_T \cdot \left(1 - \frac{1V}{V_{OVDIS}}\right)$

V_{HV} is defined thanks to R5 and R6. The resistive divider is configured as follows:

- $R_V = R5 + R6$
- $1M\Omega \leq R_V \leq 40M\Omega$
- $R5 = R_V \cdot \frac{1V}{V_{HV}}$
- $R6 = R_V \cdot \left(1 - \frac{1V}{V_{HV}}\right)$

NOTE: If ENHV = L (HVOUT is disabled), R5 and R6 are not needed, FB_HV should be left floating.

The resistors should have high values to make the current flowing through them negligible. Moreover, the following constraints must be met to ensure the functionality of the chip:

- $V_{CHRDY} + 0.05V \leq V_{OVCH} \leq 4.5V$
- $V_{OVDIS} + 0.05V \leq V_{CHRDY} \leq V_{OVCH} - 0.5V$
- $2.2V \leq V_{OVDIS}$
- $V_{HV} \leq V_{OVDIS} - 0.3V$

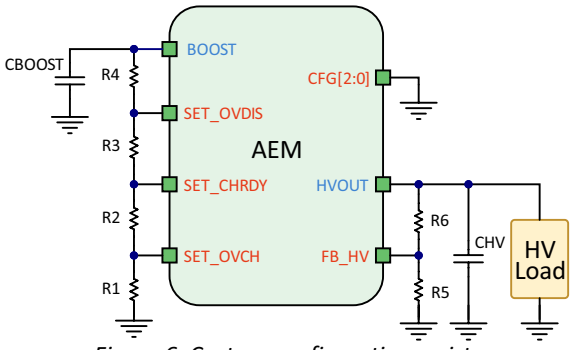

Figure 6: Custom configuration resistors

9.2. Source Voltage Configuration

To define V_{SRC_REG}, the user must configure:

- a resistive divider, as shown in Figure 7, calculated as follows:
  - $R_S = R9 + R10$
  - $100k\Omega \leq R_S \leq 1M\Omega$
  - $V_{SRC\_LVL\_U} = \frac{V_{SRC\_REG}}{Gain}$
  - $R9 = \frac{V_{SRC\_REG}}{Gain} \cdot R_S \cdot \frac{1}{2.2V}$
  - $R10 = R_S - R9$
- the SRC_LVL_RANGE[1:0] pins as shown in Table 9.

NOTE: The SRC_LVL_U voltage measure is done thanks to an Analog-to-Digital Converter (ADC) with a 27.5 mV resolution. When the measured voltage falls between two values, the higher of the two values is used as $V_{SRC\_LVL\_U}$ for V_{SRC_REG} regulation.

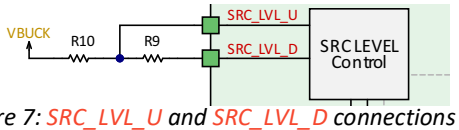

Figure 7: SRC_LVL_U and SRC_LVL_D connections

Configuration pins		
SRC_LVL_RANGE[1:0]	**Gain**	**V_{SRC_REG} range**
LL	x1	$V_{SRC\_REG} < 1.35$ V
LH	x2	1.35 V $< V_{SRC\_REG} < 2.70$ V
HL	x4	2.70 V $< V_{SRC\_REG} < 4.47$ V
HH		

Table 9: SRC_LVL_RANGE[1:0] configuration

9.3. Primary Battery Configuration

To use the primary battery, it is mandatory to determine $V_{PRIM,MIN}$, the voltage at which the primary battery is considered as fully depleted. The circuit uses a resistive divider between BUCK and FB_PRIM_D to define the voltage on FB_PRIM_U as $V_{PRIM,MIN}$ divided by 4. During $V_{PRIM,MIN}$ evaluation, the circuit connects FB_PRIM_D to GND.

When $V_{PRIM,MIN}$ is not evaluated, FB_PRIM_D is left floating to avoid quiescent current on the resistive divider. The resistors are calculated as follows:

- $R_P = R7 + R8$
- $100k\Omega \leq R_P \leq 500k\Omega$
- $R7 = \frac{V_{PRIM\_MIN}}{4} \cdot R_P \cdot \frac{1}{2.2V}$
- $R8 = R_P - R7$

NOTE: FB_PRIM_U, FB_PRIM_D and PRIM must be tied to GND if no primary battery is used.

9.4. No-battery Configuration

If the application doesn't use a storage element, the PCB must include a capacitor on the BATT pin. See Section 9.6 for C_{BATT} value.

The storage element may not be necessary in the following cases:

- If the harvested energy source is permanently available and covers the application purposes.
- If the application does not need to store energy when the harvested energy source is not available.

9.5. Supplying an Application Circuit with BUCK

It is possible to supply an application circuit directly from BUCK, with the benefit of high BATT to BUCK efficiency, provided that the following conditions are met:

- The application circuit can be supplied from a voltage in the 2.0 V - 2.5 V range (V_{BUCK} is typically 2.2 V with ripple, see Table 5).
- The sum of the following currents must be below the maximum I_{BUCK} value (see Table 5):
  - Current of the load connected to BUCK.
  - Current of the load connected to LVOUT.
- The application circuit on BUCK does not pull current during the AEM0094x cold start.

To satisfy the last condition, the following circuit may be implemented:

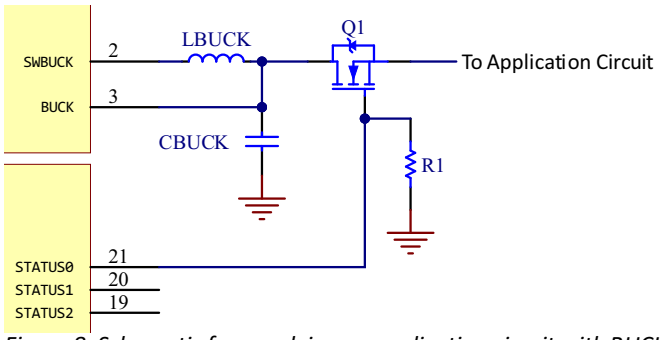

Figure 8: Schematic for supplying an application circuit with BUCK

Q1 is a N-MOSFET, whose gate is driven by STATUS[0] with R1 as a pull-down resistor. When the AEM0094x is in DEEP SLEEP MODE or in WAKE-UP MODE, STATUS[0] is LOW (see Section 8.2), ensuring that Q1 is non-conducting, and thus that the application circuit is not supplied.

When the AEM0094x switches from WAKE-UP MODE to NORMAL MODE, STATUS[0] is HIGH, making Q1 conducting. The application circuit is then supplied by BUCK, and remains so when the AEM0094x is in NORMAL MODE, OVERCHARGE MODE, PRIMARY BATTERY MODE and SHUTDOWN MODE.

Q1 must be chosen as follows:

- Low Gate-Source Leakage I_{GSS}.
- Low Zero Gate Voltage Drain Current I_{DSS}.
- Drain-Source On-State Resistance $R_{DS(on)}$ low enough to supply application circuit with an acceptable voltage drop.
- V_{GS} maximum voltage must be above V_{OVCH} (STATUS[0] HIGH voltage is V_{BOOST}).
- Maximum gate-source threshold voltage $V_{GS(th),MAX}$ matches the following, with $V_{BUCK,MAX}$ being V_{BUCK} maximum value stated in Table 5:

$$V_{GS(th),MAX} < V_{OVDIS} - V_{BUCK,MAX}$$

9.6. Storage Element Information

The energy storage element of the AEM0094x can be a rechargeable battery, a supercapacitor or a large capacitor. It should be chosen so that its voltage does not fall below V_{OVDIS} even during occasional peaks of the load current. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to buffer the battery by decoupling it with a capacitor.

The BATT pin, connecting the storage element, must never be left floating. If the application expects a disconnection of the battery (e.g., because of a user removable connector), the PCB must include a capacitor:

- If the LDOs are used, the minimum needed capacitor value is 150 µF.
- If the LDOs are not used, the minimum needed capacitor value is 22 µF.

The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the subsystem.

9.7. External Inductors Information

The AEM0094x operates with two standard miniature inductors. Switching frequency must be at least 10 MHz for both. Low equivalent series resistance (ESR) favors the power conversion efficiency of the boost and buck converters.

L_{BOOST}

The AEM0094x circuit is typically implemented with one of the following values on L_{BOOST}:

- AEM00940:
  - 10 µH (peak current min. 250 mA) allows higher current from SRC to BATT.
  - 22 µH (peak current min. 115 mA) allows better efficiencies, especially at low SRC voltages.
- AEM00941: 100 µH (peak current min. 25mA) allows for higher efficiency at the expense of lower current driving capability.

L_{BUCK}

The buck inductor L_{BUCK} must sustain a peak current of at least 50 mA. The recommended value is 10 µH.

9.8. External Capacitors Information

The AEM0094x operates with:

- Four identical standard miniature ceramic capacitors of 10 µF.
- One miniature ceramic capacitor of 22 µF.

The leakage current of the capacitors should be small as leakage currents directly impact the quiescent current of the subsystem.

C_{SRC}

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage fluctuations of V_{SRC} when the boost converter is switching. The recommended value is 10 µF +/- 20%.

C_{BUCK}

This capacitor acts as an energy buffer for the buck converter. It also reduces the voltage ripple induced by the current pulses inherent to the switching mode of the converter. The recommended value is 10 µF +/- 20%.

C_{BOOST}

This capacitor acts as an energy buffer for the boost converter. It also reduces the voltage ripple induced by the current pulses inherent to the switching mode of the converter. The recommended value is 22 µF +/- 20%.

C_{HV} / C_{LV}

These capacitors ensure a high-efficiency load regulation of the high-voltage and low-voltage LDO regulators. Closed-loop stability requires the value to be in the range of 8 µF to 14 µF.

10. Typical Application Circuits

10.1. Example Circuit 1

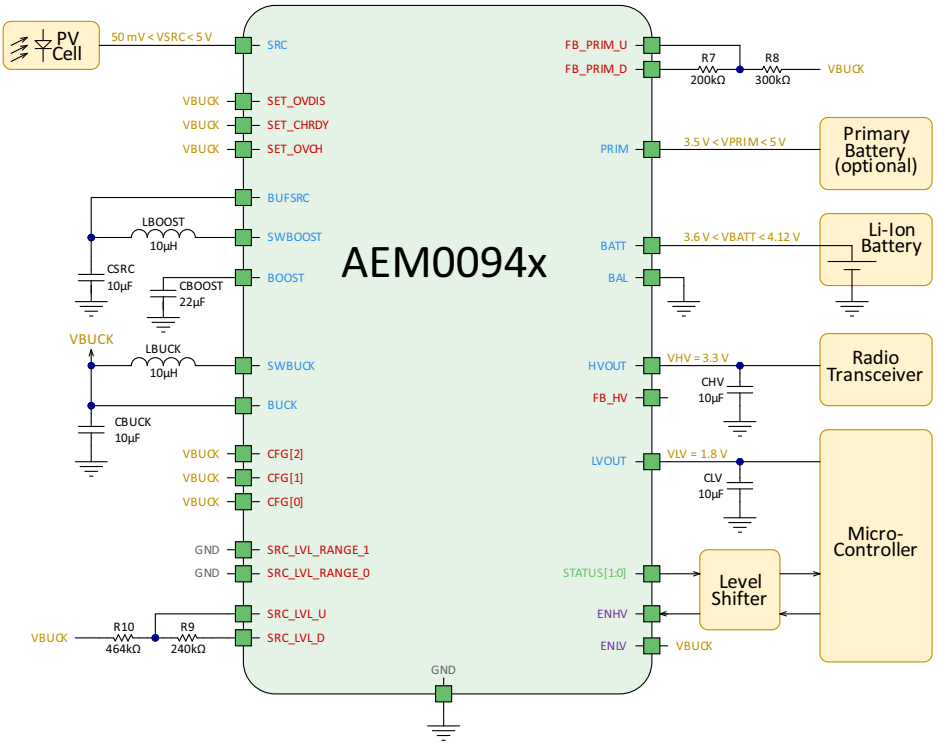

Figure 9: Typical application circuit 1

The energy source is a photovoltaic cell and the storage element is a standard Li-ion battery cell. The radio communication is supplied by HVOUT set at 3.3 V. The micro-controller that controls the application is supplied by LVOUT set at 1.8 V.

This circuit uses a pre-defined AEM configuration, typical of systems that use standard components for radio and energy storage.

The operating mode pins are set as follows:

- CFG[2:0] = HHH (all to V_{BUCK})

Referring to Table 8, in this mode, the threshold voltages are:

- V_{OVCH} = 4.12 V
- V_{CHRDY} = 3.67 V
- V_{OVDIS} = 3.60 V

Moreover, the LDOs output voltages are:

- V_{HV} = 3.3 V
- V_{LV} = 1.8 V

A primary battery is also connected as a back-up solution. The minimal level allowed on this battery is set at 3.5 V. Following equations from Section 9.3:

- $R_P = 0.5M\Omega$
- $R7 = \frac{3.5V}{4} \cdot 0.5M\Omega \cdot \frac{1}{2.2V} = 200k\Omega$
- $R8 = 0.5M\Omega - 200k\Omega = 300k\Omega$

The PV cell used needs a constant source voltage regulation at 0.75 V to extract the maximum power regardless of the brightness. SRC_LVL_RANGE[1:0] is set to LL according to Table 9.

- $R_S = 704k\Omega$
- $R9 = \frac{0.75}{1} \cdot 704k\Omega \cdot \frac{1}{2.2V} = 240k\Omega$
- $R10 = 704k\Omega - 240k\Omega = 464k\Omega$

The LVOUT LDO output is enabled by tying ENLV to BUCK.

The micro-controller is supplied by LVOUT, that is enabled when V_{BATT} and V_{BOOST} voltage rise above V_{CHRDY}.

The application software can enable or disable the radio transceiver supply with a GPIO connected to ENHV.

10.2. Example Circuit 2

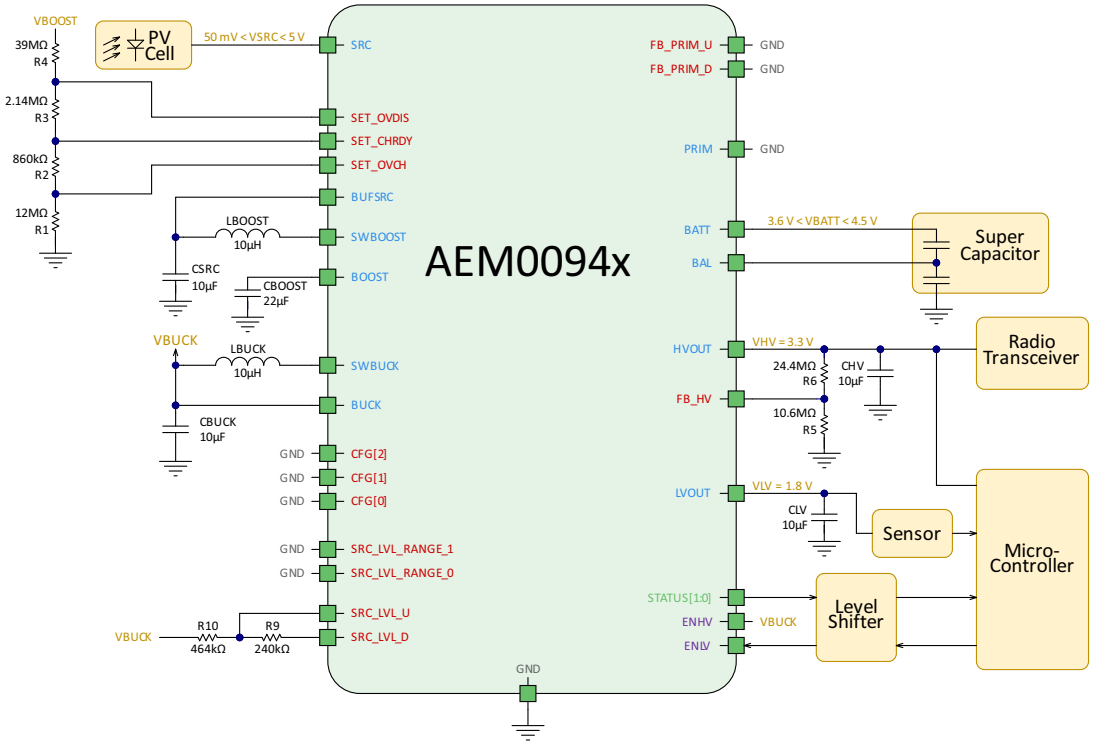

Figure 10: Typical application circuit 2

The energy source is a photovoltaic cell and the storage element is a dual-cell supercapacitor. Please note that the supercapacitor might be completely depleted during the cold start.

Moreover, BAL is connected to the dual-cell supercapacitor to compensate for any mismatch between the two cells and, in that way, protect the supercapacitor.

A micro-controller acts as the application master. The operating mode pins are set as follows:

- CFG[2:0] = LLL (all to GND)

The storage element voltages are set as follows with a custom configuration:

- V_{OVCH} = 4.5 V
- V_{CHRDY} = 4.2 V
- V_{OVDIS} = 3.6 V

R_T is set to 54 MΩ. R1, R2, R3 and R4 values are computed from the equations in Section 9.1.1:

- $R1 = 54M\Omega \cdot \frac{1V}{4.5V} = 12M\Omega$
- $R2 = 54M\Omega \cdot \left(\frac{1V}{4.2V} - \frac{1V}{4.5V}\right) = 860k\Omega$
- $R3 = 54M\Omega \cdot \left(\frac{1V}{3.5V} - \frac{1V}{4.2V}\right) = 2.14M\Omega$
- $R4 = 54M\Omega \cdot \left(1 - \frac{1V}{3.5V}\right) = 39M\Omega$

The LDO voltages are set as follows:

- V_{HV} = 3.3 V
- V_{LV} = 1.8 V

Enabling and disabling LVOUT is controlled by the application circuit with a micro-controller GPIO connected to ENLV.

ENHV is tied to BUCK so that HVOUT is always on.

R_V is set to 35 MΩ. R5 and R6 are determined by applying the equations found in Section 9.1:

- $R5 = 35M\Omega \cdot \frac{1V}{3.3V} = 10.6M\Omega$
- $R6 = 35M\Omega \cdot \left(1 - \frac{1V}{3.3V}\right) = 24.4M\Omega$

The micro-controller is supplied by HVOUT, which is enabled when V_{BATT} and V_{BOOST} voltages rise above V_{CHRDY}.

The photovoltaic cell used needs a constant source voltage regulation at 0.75 V to provide the maximum power regardless of the ambient luminosity. SRC_LVL_RANGE[1:0] is set to LL according to the Table 9.

- $R_S = 704k\Omega$
- $R9 = \frac{0.75}{1} \cdot 704k\Omega \cdot \frac{1}{2.2V} = 240k\Omega$
- $R10 = 704k\Omega - 240k\Omega = 464k\Omega$

No primary battery is connected: PRIM, FB_PRIM_U and FB_PRIM_D pins are tied to GND.

11. Circuit Behavior

11.1. Cold-start Behavior

11.1.1. (Super)capacitor as a Storage Element

The following figure shows the AEM0094x behavior with a capacitor connected to BATT and the following settings:

- CFG[2:0] = LHH
- $V_{SRC,REG}$ = 2.1 V
- C_{BATT} = 4.85 mF
- SRC: 1 mA current source with 3 V voltage compliance
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT

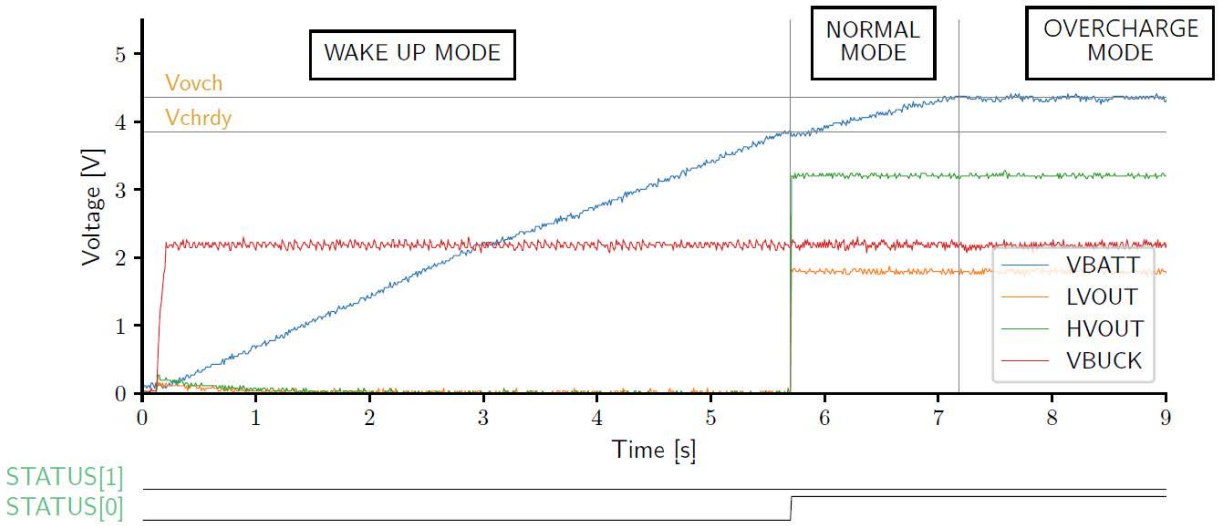

Figure 11: Cold start with a capacitor connected to BATT

11.1.2. Battery as a Storage Element

The following figure shows the AEM0094x behavior with a pre-charged capacitor (acting as a battery) connected to BATT and the following settings:

- CFG[2:0] = LHH
- $V_{SRC,REG}$ = 2.1 V
- C_{BATT} = 4.85 mF
- SRC: 1 mA current source with 3 V voltage compliance
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT

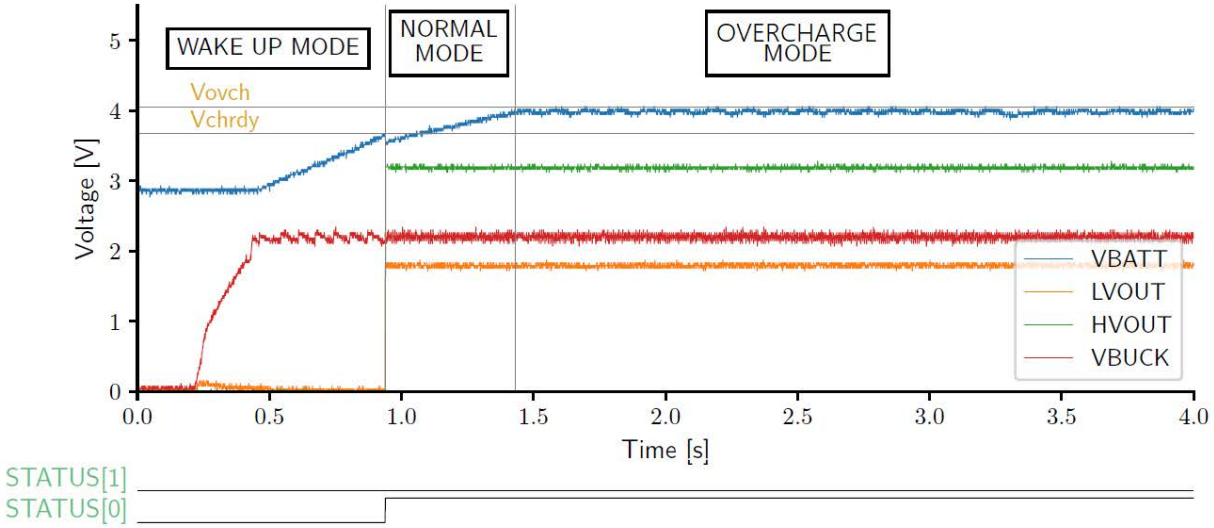

Figure 12: Cold start with a battery connected to BATT

11.2. Overcharge Mode Behavior

The following figure shows the AEM0094x behavior in OVERCHARGE MODE with the following settings:

- CFG[2:0] = HHH
- $V_{SRC,REG}$ = 2.1 V
- C_{BATT} = 4.85 mF
- SRC: 1 mA current source with 3 V voltage compliance
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT

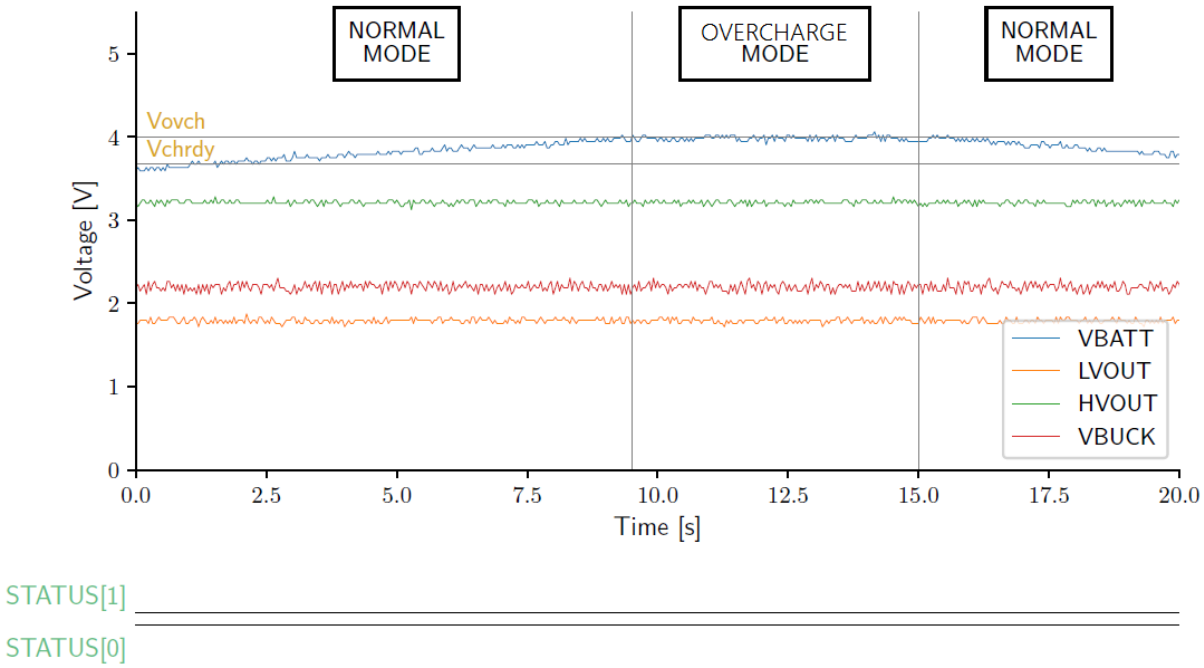

Figure 13: Overcharge mode

11.3. Shutdown Mode Behavior

11.3.1. Without Primary Battery

The following figure shows the AEM0094x behavior in SHUTDOWN MODE with the following settings:

- CFG[2:0] = LHL
- $V_{SRC,REG}$ = 2.1 V
- C_{BATT} = 4.85 mF
- SRC: left floating to let the storage element on BATT discharge
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 22 kΩ resistive load on HVOUT
- PRIM, FB_PRIM_U and FB_PRIM_D connected to GND

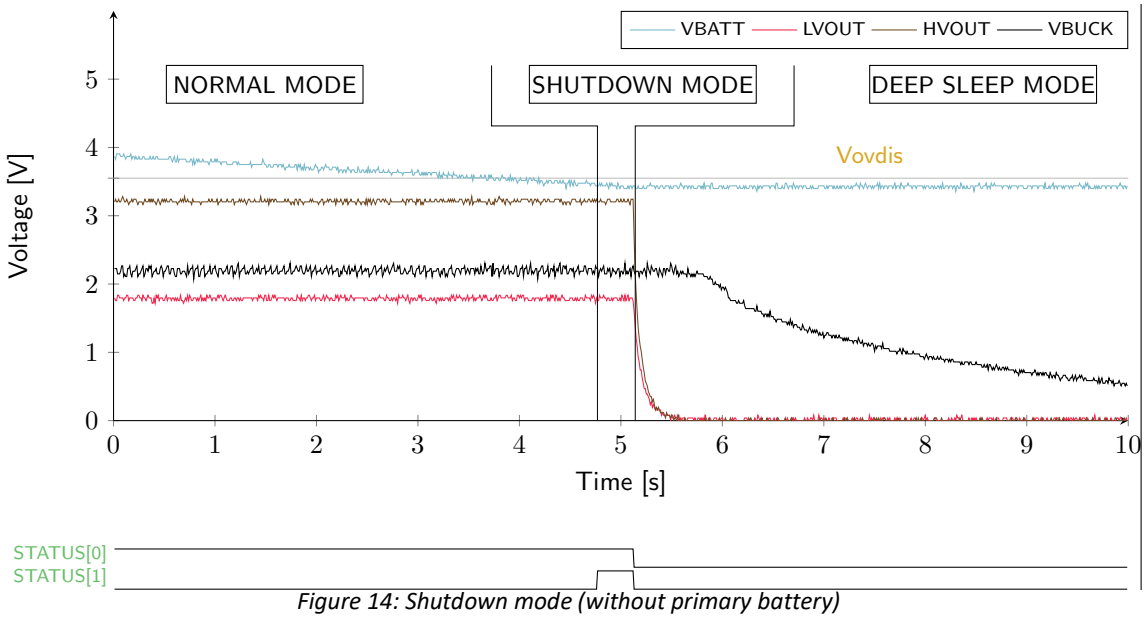

Figure 14: Shutdown mode (without primary battery)

11.3.2. With Primary Battery

The following figure shows the AEM0094x behavior in SHUTDOWN MODE with the following settings:

- CFG[2:0] = HHH
- $V_{SRC,REG}$ = 2.1 V
- C_{BATT} = 4.85 mF
- SRC: left floating to let the storage element on BATT discharge
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 22 kΩ resistive load on HVOUT
- PRIM: 3 V voltage source with 1 mA current compliance
- R7 = 68 kΩ
- R8 = 330 kΩ

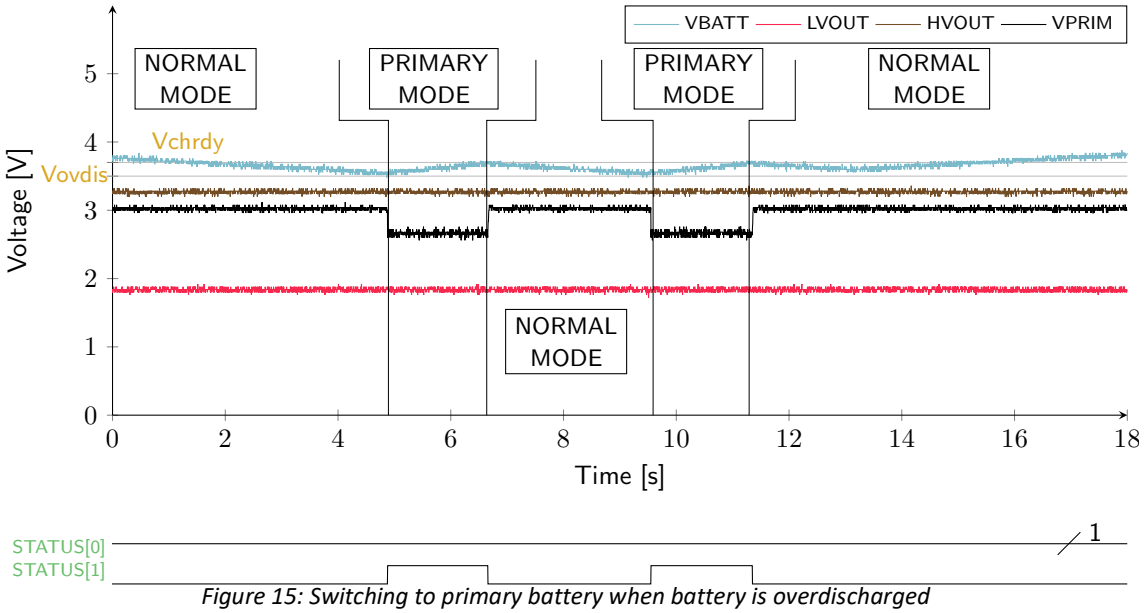

Figure 15: Switching to primary battery when battery is overdischarged

12. Performance Data

12.1. BOOST Conversion Efficiency for LBOOST = 10 µH

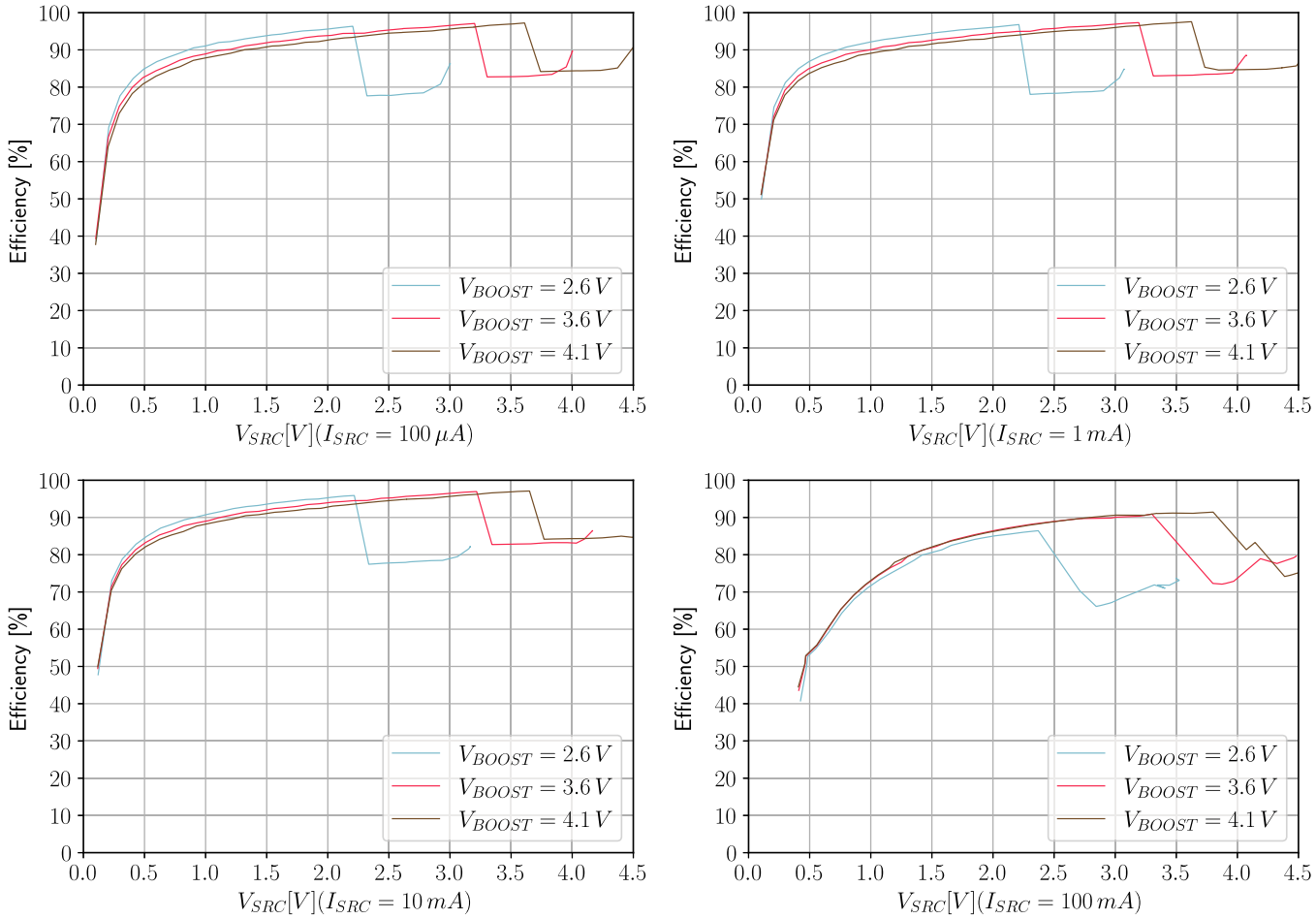

Figure 16: Boost efficiency for Isrc: 100µA, 1mA, 10mA and 100mA (AEM00940 LBOOST = 10 µH)

12.2. BOOST Conversion Efficiency for LBOOST = 22 µH

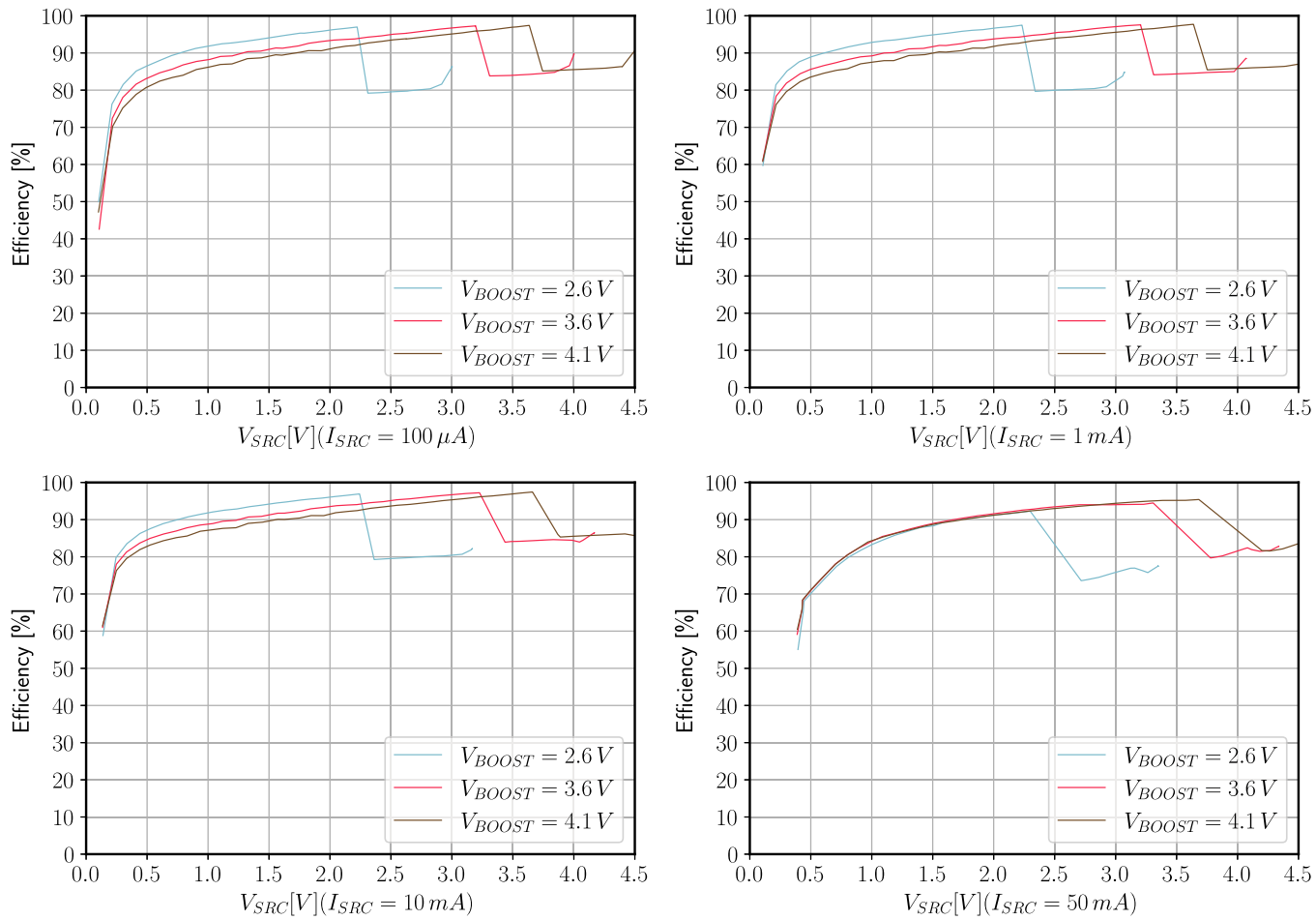

Figure 17: Boost efficiency for Isrc: 100µA, 1mA, 10mA and 50mA (AEM00940 LBOOST = 22 µH)

12.3. BOOST Conversion Efficiency for LBOOST = 100 µH

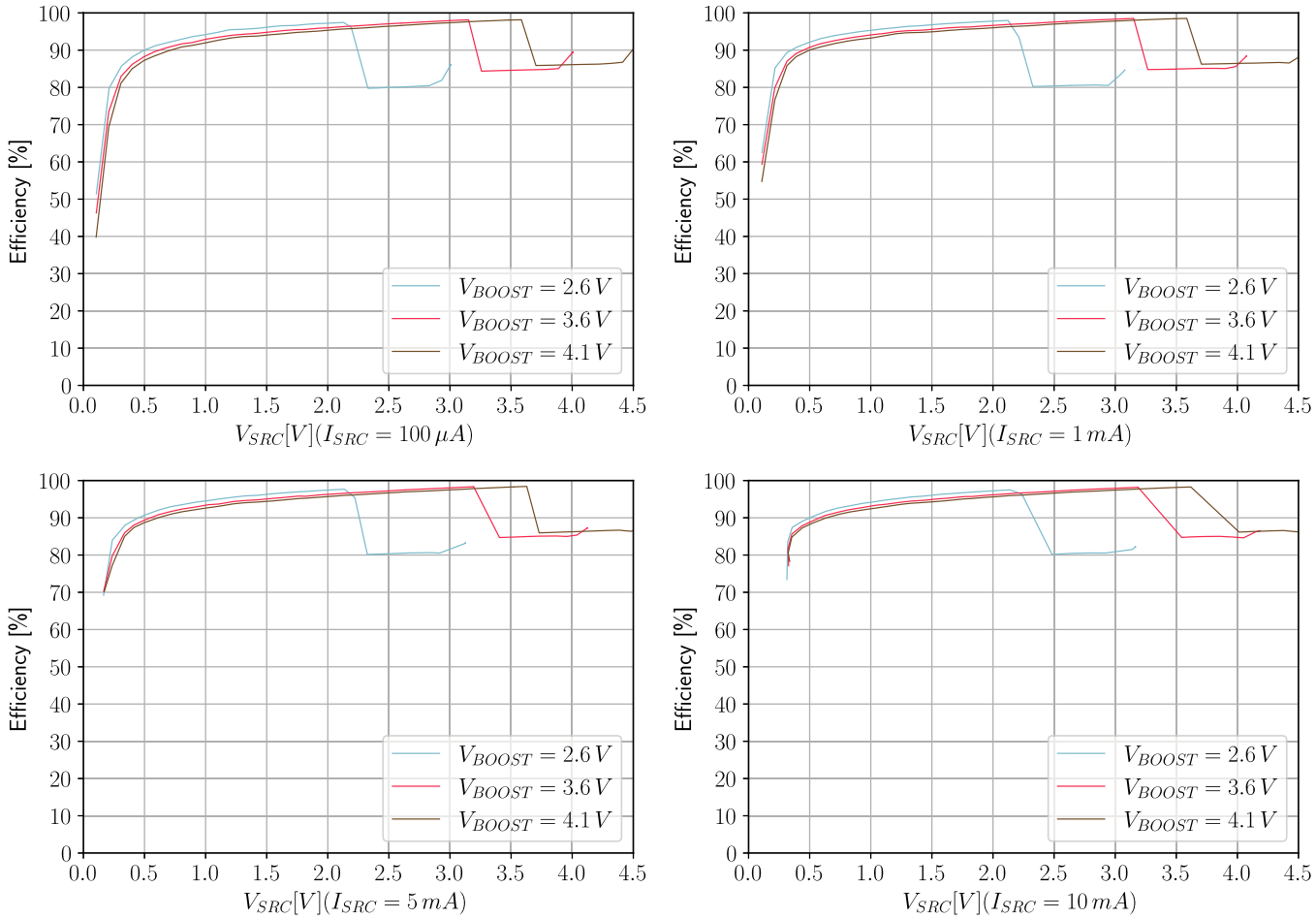

Figure 18: Boost efficiency for Isrc: 100µA, 1mA, 5mA and 10mA (AEM00941 LBOOST = 100 µH)

12.4. BUCK Conversion Efficiency

The following graph shows the buck converter efficiency from BATT to BUCK with the AEM0094x quiescent current I_Q subtracted.

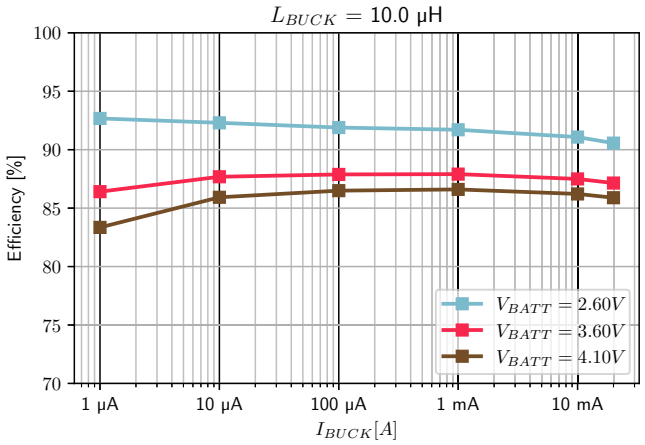

Figure 19: Buck Efficiency (L_{BUCK} = 10 µH)

12.5. Quiescent Current

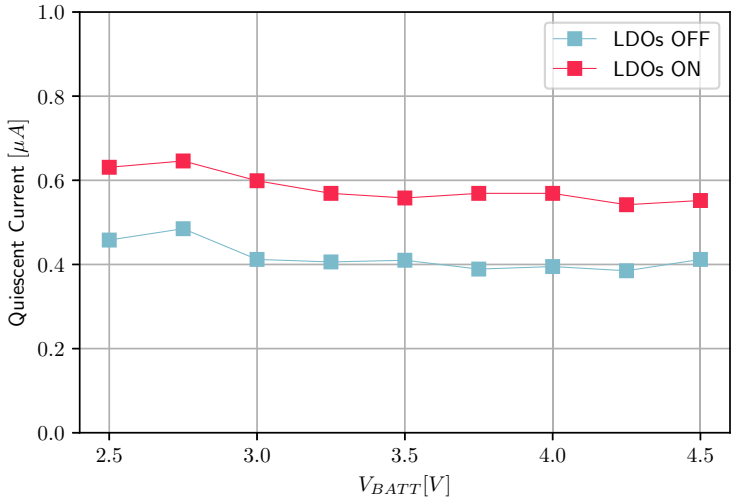

Figure 20: Quiescent current with LDOs on and off

12.6. High-voltage LDO Regulation

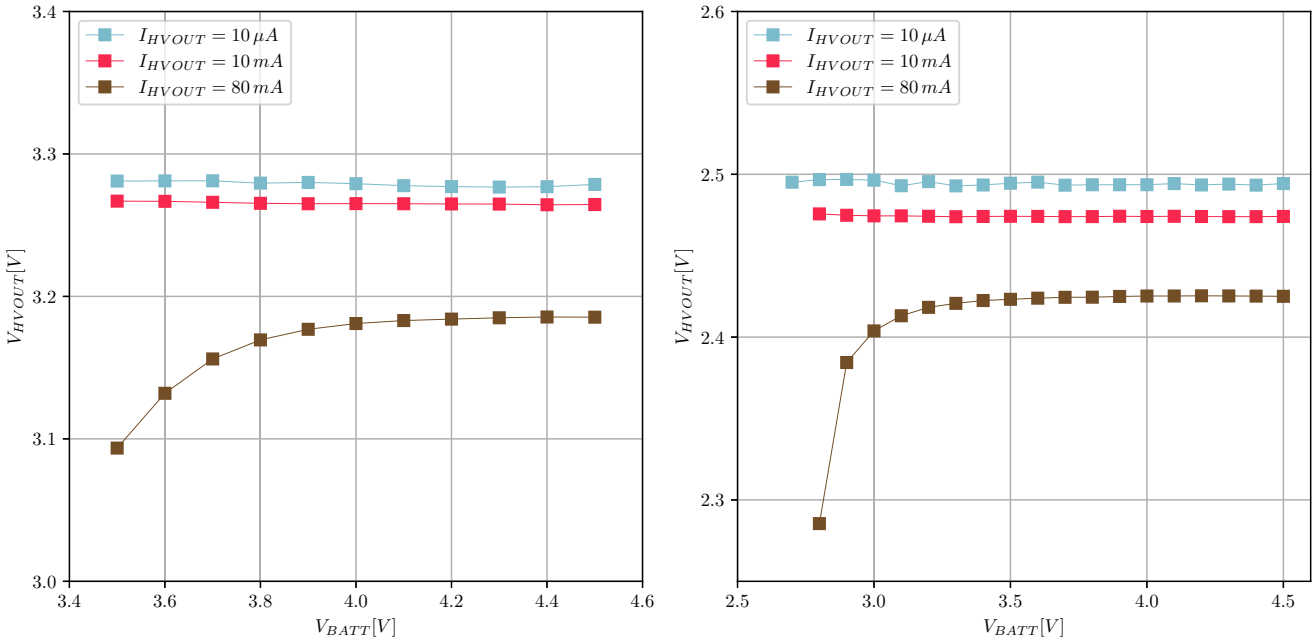

Figure 21: HVOUT at 3.3 V and 2.5 V

12.7. Low-voltage LDO Regulation

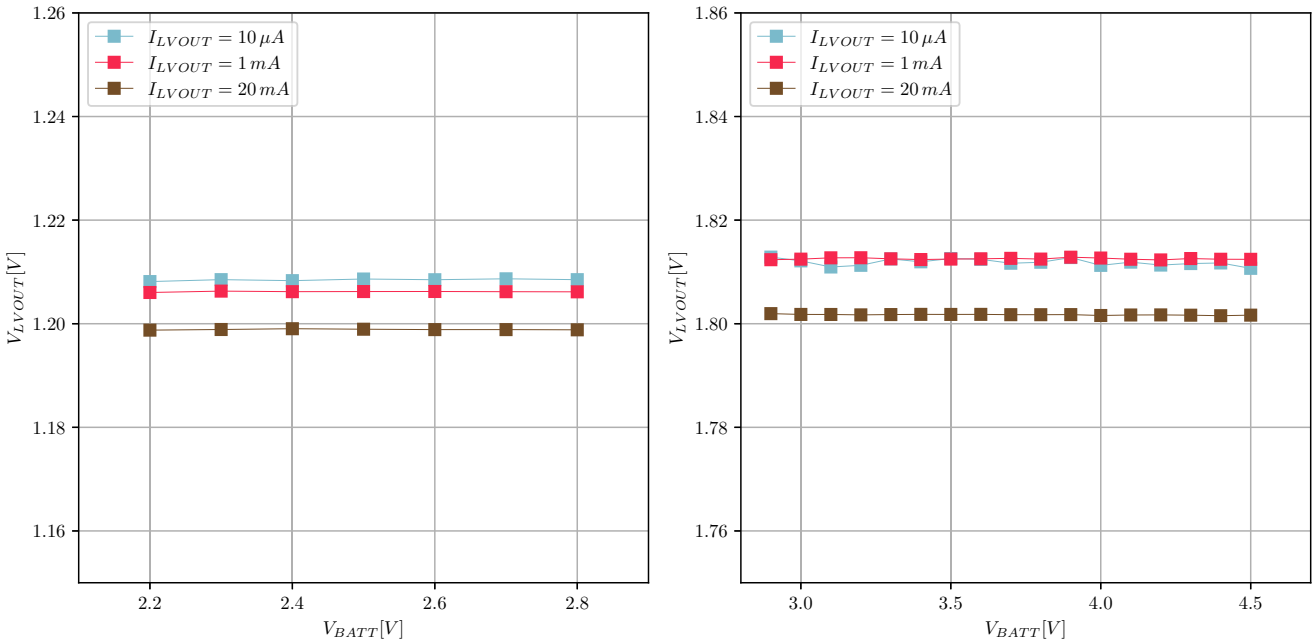

Figure 22: LVOUT at 1.2 V and 1.8 V

12.8. High-voltage LDO Efficiency

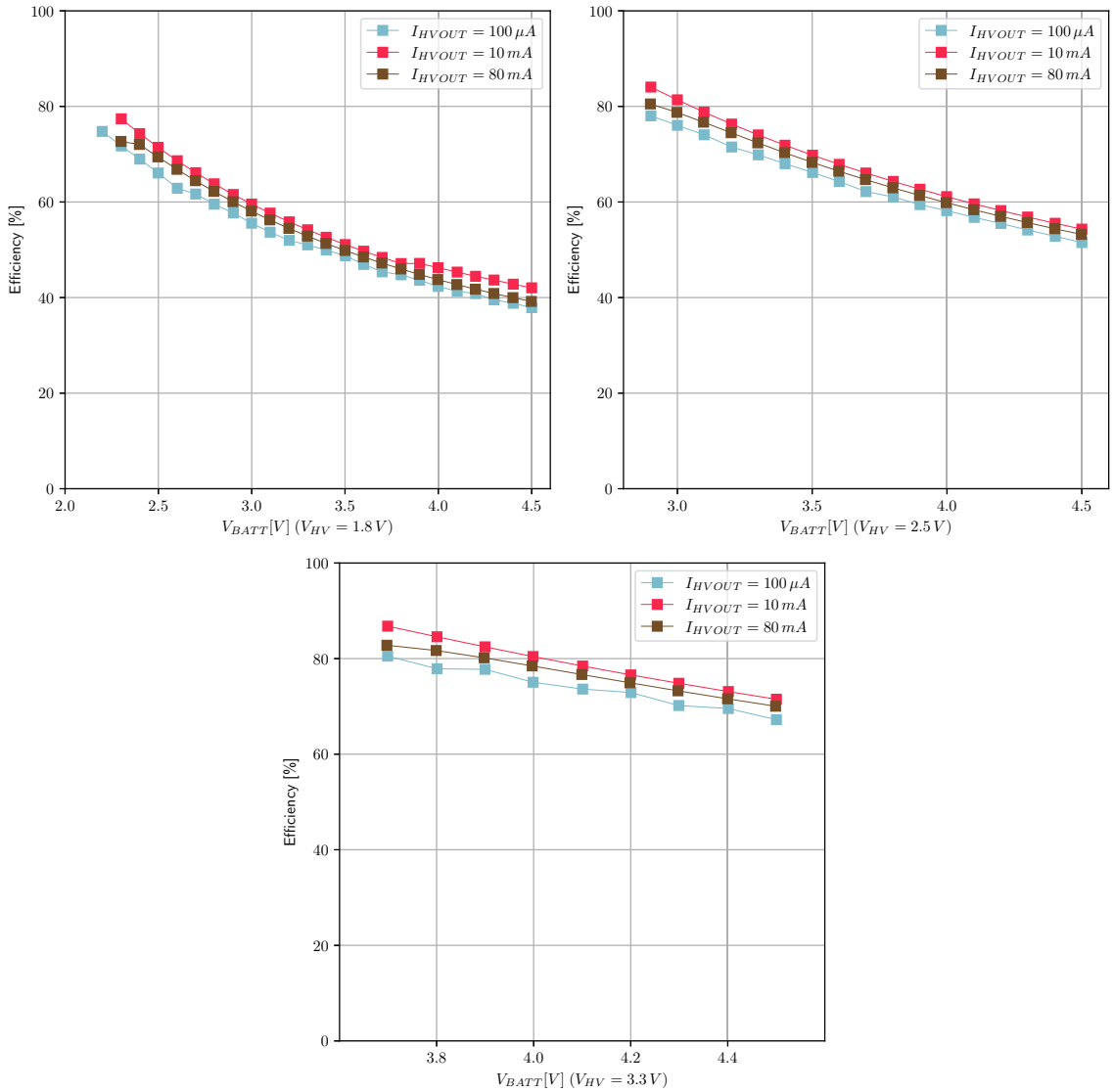

Figure 23: HVOUT efficiency at 1.8V, 2.5V and 3.3 V

The theoretical efficiency of an LDO can be calculated as Vout / Vin if quiescent current can be neglected with regards to the output current. For the high-voltage LDO, the theoretical efficiency is equal to V_{HV} / V_{BATT}.

12.9. Low-voltage LDO Efficiency

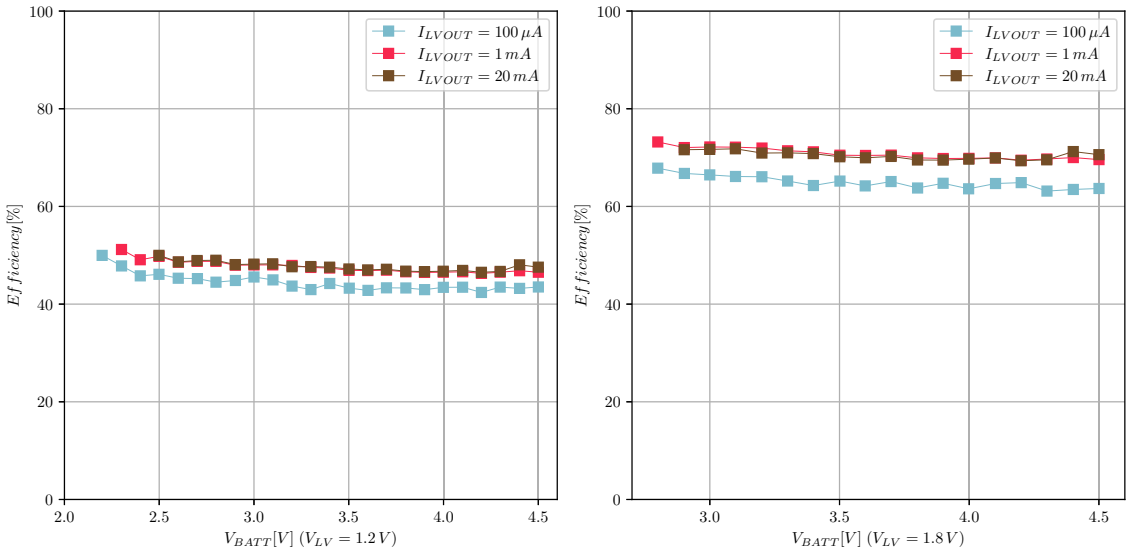

Figure 24: Efficiency of buck cascaded with LVOUT at 1.2 V and 1.8 V

The theoretical efficiency of an LDO can be calculated as V_{LV} / V_{BUCK}. Starting from the battery, the efficiency of the buck converter (ηbuck) has to be taken into account (see Figure 4).

The efficiency between V_{BATT} and V_{LV} is therefore equal to:

$$\eta_{BUCK} \cdot \frac{V_{LV}}{V_{BUCK}}$$

13. Schematic

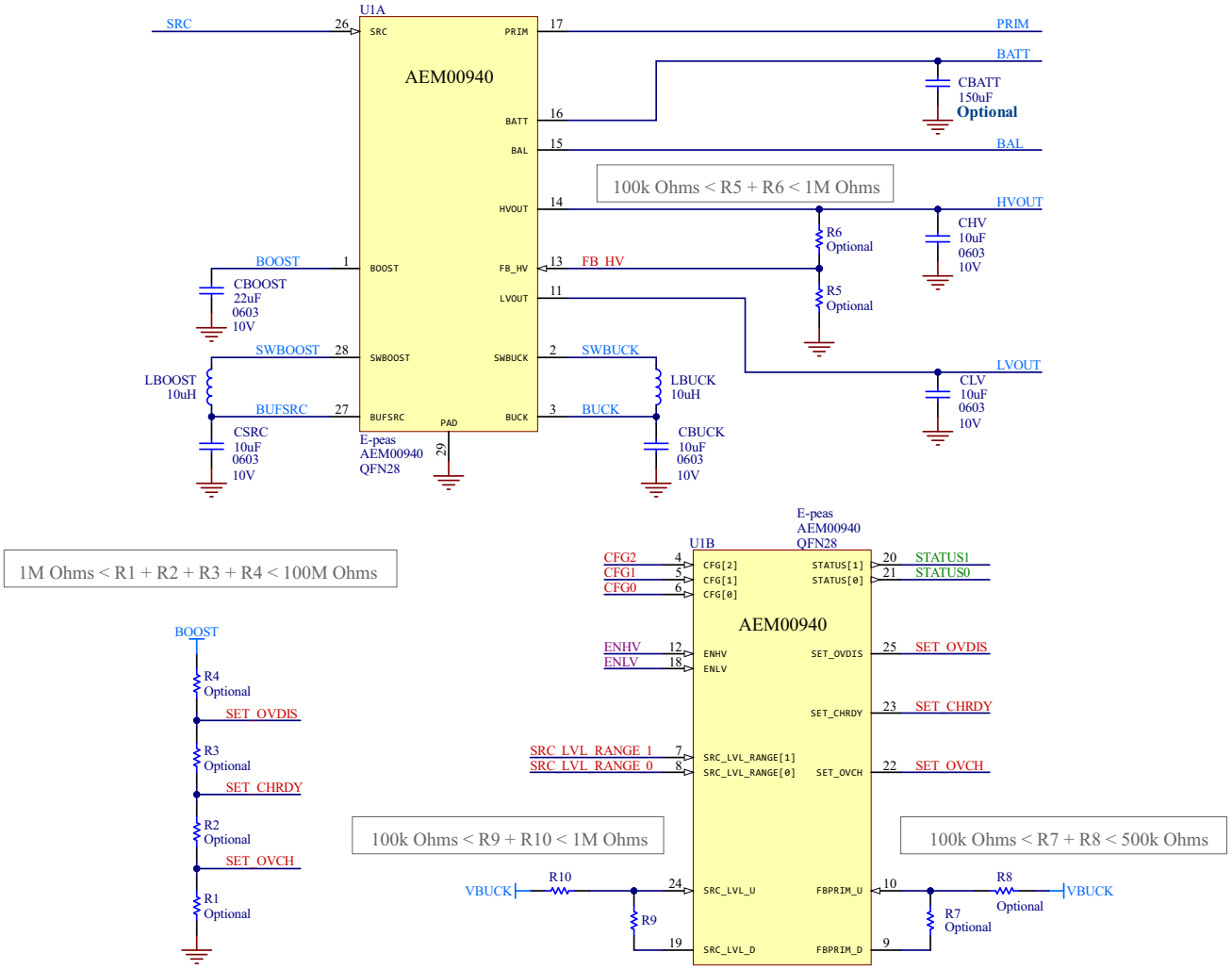

Figure 25: Schematic example

Designator	Description	Quantity	Manufacturer	Part Number
U1	AEM0094x	1	e-peas	order at sales@e-peas.com
For AEM00940:				
L_{BOOST}	Power Inductor 10 µH - 0,90 A - LPS4018	1	Coilcraft	LPS4018-103MR
L_{BOOST} (alt.)	Power Inductor 10 µH - 0,84 A - 3015	1	Würth	744 040 321 00
L_{BOOST} (alt.)	Power Inductor 22 µH - 0,65 A - LPS4018	1	Coilcraft	LPS4018-223MR
For AEM00941:				
L_{BOOST}	Power Inductor 100 µH - 0,55 A - LPS5030	1	Coilcraft	LPS5030-104MR
C_{BOOST}	Ceramic Cap 22 µF, 10 V, 20%, X5R, 0603	1	Murata	GRM188R61A226ME15D
L_{BUCK}	Power Inductor 10 µH - 0,25 A - 0603	1	TDK	MLZ1608M100WT
C_{BUCK}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{SRC}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{HV}	Ceramic Cap 10 µF, 25 V, 10%, X7S, 0805	1	TDK	C2012X7S1E106K125AE
C_{LV}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{BATT}	Ceramic Cap 150 µF, 6.3 V, 20%, X5R, 1206	1	TDK	GRM31CR60J157ME11L

Table 10: BOM example for AEM0094x and its required passive components

14. Layout

14.1. Guidelines

Good layout practices are mandatory in order to obtain good AEM0094x stability, best efficiency and avoid EMI problems.

The following list, while not exhaustive, shows the main attention points when routing a PCB with the AEM0094x:

- The switching nodes (BUFSRC, SWBOOST, SWBUCK and BUCK) must be kept as short as possible, with minimal track resistance and minimal track capacitance. Low resistance is obtained by keeping track length as short as possible and track width as large as possible between these switching nodes and the AEM0094x pins. Minimal capacitance is obtained by maintaining a large distance between the switching nodes and other signals. We recommend removing the ground plane, the power plane and the bottom layer ground pour under L_{BOOST} and L_{BUCK} footprints, as well as adding distance between BUFSRC/SWBOOST and the top ground pour, as shown in Figure 26.
- The decoupling capacitors (C_{BOOST} - C_{BUCK} - C_{SRC} - C_{HV} - C_{LV} - C_{BATT}) must be placed as close as possible to the AEM0094x, with direct connection and minimum track resistance for the corresponding power nodes (BOOST, BUCK, BUFSRC, HVOUT, LVOUT and BATT).
- The GND return path between the decoupling capacitors and the AEM0094x thermal pad, which is the AEM0094x main GND connection, must be as direct and short as possible. This is preferably done on the top layer when possible, otherwise by internal/bottom plane, using low resistance vias to decrease layer-to-layer connection resistance. In Figure 26, this GND return path is done on an internal plane.
- The external DC power connections (SRC, HVOUT, LVOUT and BATT) must be connected to the AEM0094x with low resistance tracks.
- The BAL pin connection track must be able to handle at least 40 mA.
- The custom mode setting pins SET_OVDIS, SET_CHRDY and SET_OVCH are high impedance analog inputs typically connected to a resistive divider with high resistor values, making those three nodes prone to pickup noise. Thus, it is recommended to keep those as short as possible and as far as possible to noise sources such as DCDC switching nodes.
- The configuration pins and the status pins have minimal layout restrictions.

14.2. Layout Example

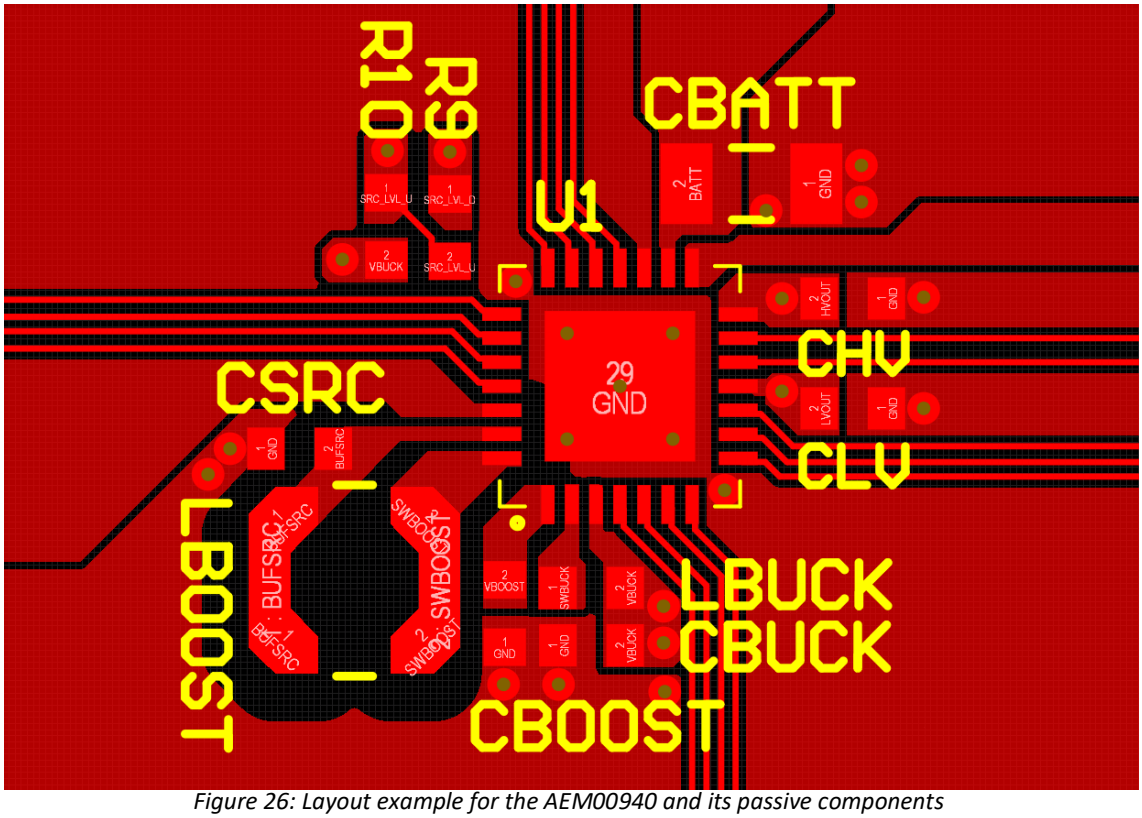

Figure 26: Layout example for the AEM00940 and its passive components

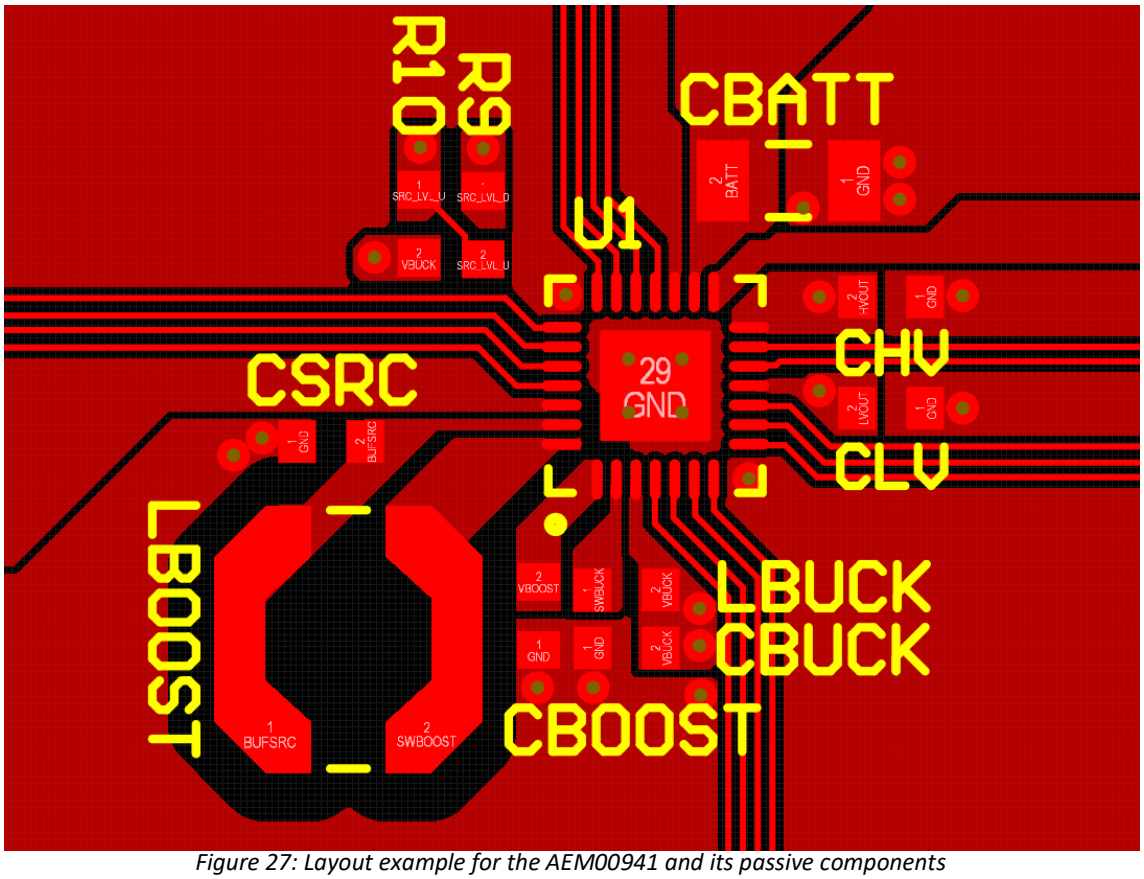

Figure 27: Layout example for the AEM00941 and its passive components

15. Package Information

15.1. Plastic Quad Flatpack No-lead (QFN 28-pin 5x5mm)

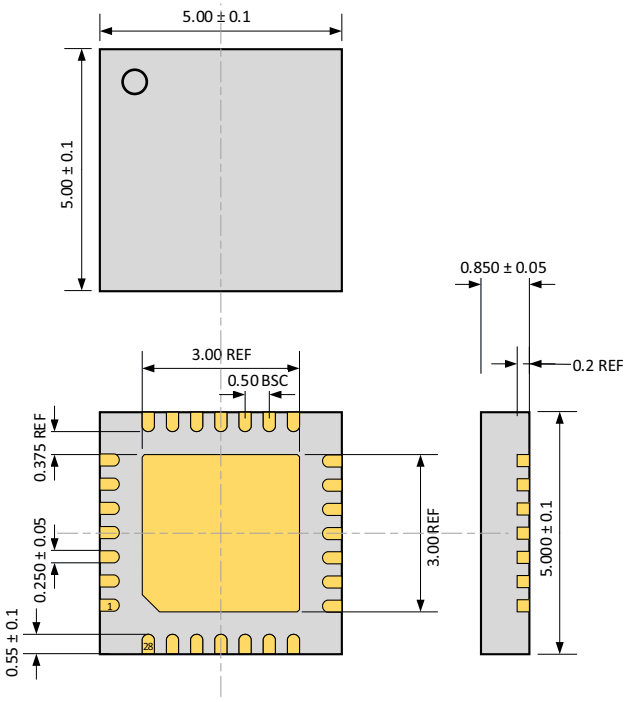

Figure 28: QFN 28-pin 5x5mm drawing (all dimension in mm)

15.2. Board Layout (QFN 28-pin 5x5mm)

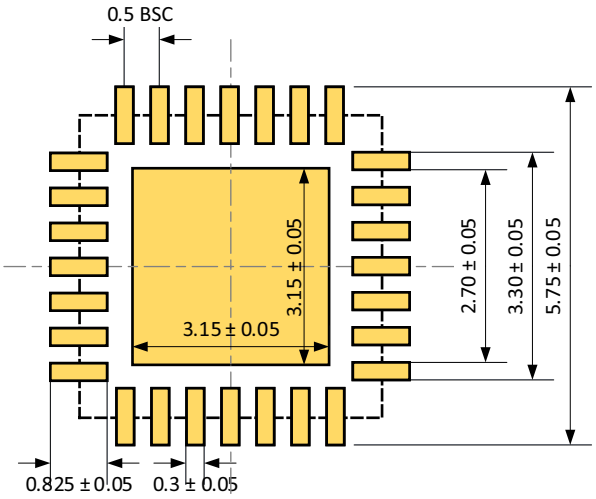

Figure 29: Recommended board layout for QFN 28-pin 5x5mm (all dimension in mm)

15.3. Plastic Quad Flatpack No-lead (QFN 28-pin 4x4mm)

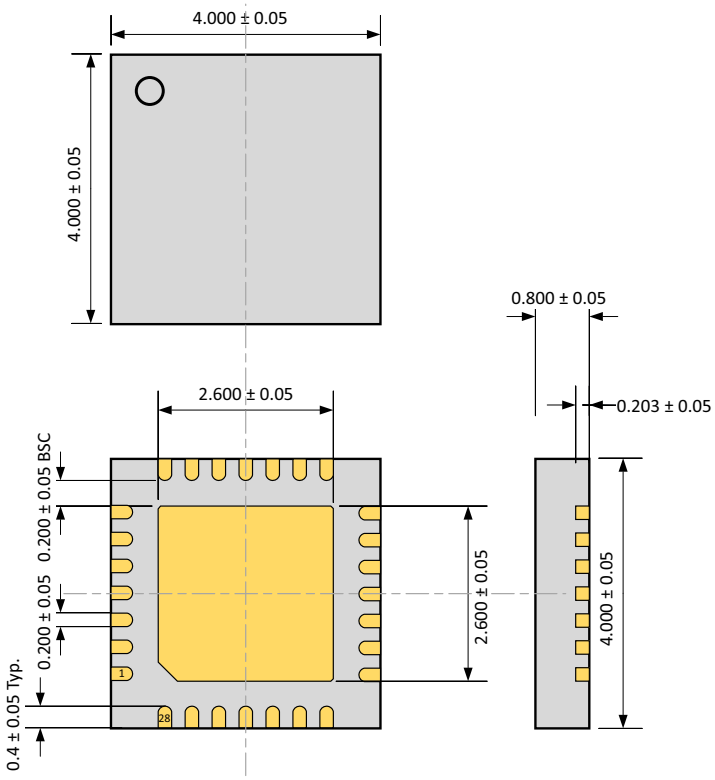

Figure 30: QFN 28-pin 4x4mm drawing (all dimension in mm)

15.4. Board Layout (QFN 28-pin 4x4mm)

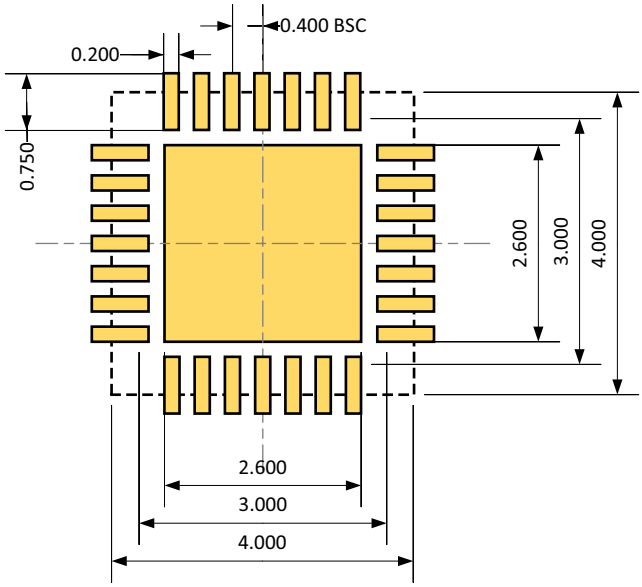

Figure 31: Recommended board layout for QFN 28-pin 4x4mm (all dimension in mm)

16. Glossary

AEM

Ambient Energy Manager.

BOM

Bill Of Materials.

C_{BATT}

Capacitor connected on the BATT pin (if no storage element connected).

C_{BOOST}

Output capacitor of the BOOST converter.

C_{BUCK}

Output capacitor of the BUCK converter.

C_{HV}

High-voltage LDO regulator decoupling capacitor.

C_{LV}

Low-voltage LDO regulator decoupling capacitor.

C_{SRC}

BUFSRC pin decoupling capacitor.

GPIO

General Purpose Input / Output.

I_{BUCK}

Total load current supplied by the BUCK converter (including the LVOUT current I_{LV}).

I_{HV}

Load current supplied by the high-voltage LDO regulator.

I_{LV}

Load current supplied by the low-voltage LDO regulator.

I_{PRIM}

Current from the primary battery.

I_Q

Quiescent current on BATT when no energy is available on SRC.

I_{SRC}

Harvested current from the energy source.

L_{BOOST}

BOOST converter inductor.

L_{BUCK}

BUCK converter inductor.

LDO

Low Drop-Out.

PCB

Printed Circuit Board.

P_{SRC_CS}

Minimum power available on SRC for the AEM0094x to coldstart.

R_P

Sum of resistors for setting the primary battery minimum voltage. R_P = R7 + R8.

R_S

Sum of resistors for setting the source voltage regulation. R_S = R9 + R10.

R_T

Sum of resistors for setting the battery protection threshold voltages in custom mode. R_T = R1 + R2 + R3 + R4.

R_V

Sum of resistors for setting the output voltage of the high-voltage LDO in custom mode. R_V = R5 + R6.

T_{CRIT}

Time before shutdown once STATUS[1] has been asserted.

$T_{VSRC\_REG,UPDATE}$

Time between two updates of the source voltage regulation.

V_{BATT}

Voltage on the BATT pin.

V_{BOOST}

Output voltage of the BOOST converter.

V_{BUCK}

Output voltage of the BUCK converter.

V_{CHRDY}

Charge ready voltage on the BATT pin.

$V_{FB\_PRIM\_U}$

Feedback for the minimal voltage level on the primary battery.

V_{HV}

Output voltage of the high-voltage LDO regulator.

V_{LV}

Output voltage of the low-voltage LDO regulator.

V_{OC}
: Open-circuit voltage of the harvester connected to the SRC pin.

V_{OVCH}
: Over-charge voltage on the BATT pin.

V_{OVDIS}
: Over-discharge voltage on the BATT pin.

V_{PRIM}
: Voltage on the primary battery.

$V_{PRIM,MIN}$
: Voltage at which the primary battery is considered fully depleted.

V_{SRC}
: Voltage on the SRC pin.

$V_{SRC\_LVL\_U}$
: Voltage on the SRC_LVL_U pin.

V_{SRC_REG}
: Target regulation voltage on the SRC pin.

17. Revision History

Revision	Date	Description
1.0	February, 2022	Creation of the document.

1.1	January, 2024	- AEM00941 added. AEM0094x used when both AEM00940 and AEM00941 concerned.
		- Term “Balun” replaced by “Storage Element Balancing Circuit”.
		- Term “OVERVOLTAGE mode” replaced by “OVERCHARGE mode”.
		- External component names color changed to orange instead of blue.
		- R9 and R10 swapped in the whole document.
		- First page:
		  - Input voltage range and device information added.
		  - Link to e-peas website added for evaluation boards information.
		  - Typical inductors values for LBOOST added.
		- Aesthetic changes on Figures 1, 5, 9, 10, first page figure, LDOs configuration table.
		- SET_OVDIS, SET_CHRDY and SET_OVCH pins changed from “left floating” to “connected to VBUCK” when not used (Table 1 and Section 9.1).
		- Added “Pin Configuration and Functions” section containing the pinout diagram and description.
		- Added all the missing pins in the Absolute Maximum Ratings table.
		- Electrical characteristics table:
		  - VSRC maximum value during and after cold start modified to 5 V.
		  - ISRC value added for LBOOST values of 22 µH and 100 µH.
		  - Different min values for VBATT depending on used storage element removed.
		  - VPRIM maximum value changed from 4.5 V to 5 V.
		  - VHV maximum value changed from “VBATT - 0.3 V” to “VOVDIS - 0.3 V”.
		  - Added IBUCK, TVSRC_REG.UPDATE and IQ values.
		- Recommended operating conditions table:
		  - CSRC maximum value of 22 µF added.
		  - LBOOST value of 100 µH added for the AEM00941.
		  - Inductors unit error corrected to µH.
		  - CBOOST, CBUCK and LBOOST maximum values removed.
		  - ENHV minimum and maximum values removed.
		  - ENLV minimum value replaced by VBUCK.
		- Pin names changed from “STO_OVDIS, STO_RDY and STO_OVCH” to “SET_OVDIS, SET_CHRDY and SET_OVCH” and LBOOST value removed in Functional block diagram.
		- Condition to go from SHUTDOWN mode to NORMAL mode corrected to “If VBATT > VOVDIS” in Figure 5 and Section 8.2.5.
		- Added the Source Voltage Regulation section.
		- Added how to use BUCK to supply an application, and BUCK converter performances.
		- Second CBATT value added of 22 µF when storage element not connected and LDOs not used (Section 9.6).
		- External inductors information section:
		  - Second LBOOST recommended value added for the AEM00940.
		  - LBOOST recommended value added for the AEM00941.
		- Modified VOVDIS, R2, R3 and R4 values in Example Circuit 2.
		- New “Circuit Behavior” section created to place the circuit behavior figures.
		- Changed the way of displaying the settings used for the circuit behavior figures.
		- SHUTDOWN mode behavior figures (with and without primary battery) added.
		- Added AEM00941 efficiency graphs with LBOOST = 100 µH.
		- BOM and required passive components example added.
		- Added layout guidelines section and glossary section.
		- QFN-28pin 4x4mm package information added for AEM00941.
		- Replace 0 by L for logic low and 1 by H for logic high in tables and texts.

Table 11: Revision history