

## AEM00941 Evaluation Board User Guide

### Description

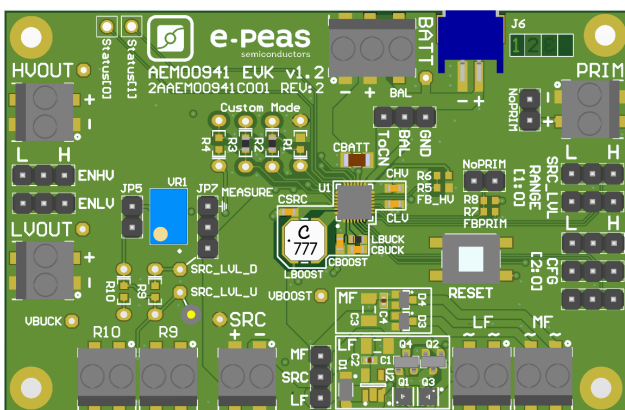
The AEM00941 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM00941 integrated circuit (IC). Please refer to the datasheet for all the useful details about the AEM00941 (Document DS\_AEM00941).

The AEM00941 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting.

It allows easy connections to the energy harvester (DC or AC source), the storage element, the low-voltage and the high-voltage loads. This evaluation board includes two rectifiers for the low and medium frequency AC sources. It also provides all the configuration access to set the device in any one of the modes described in the datasheet. The control and status signals are available on standard pin headers, allowing users to wire for any usage scenario and evaluate the relevant performance.

The AEM00941 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes...) for the design of a highly efficient subsystem powered by energy harvesting in your target application.

### Appearance



### Features

#### Two-way screw terminals

- Source of energy (DC).
- Source of energy (low frequency AC).
- Source of energy (medium frequency AC).
- Low-voltage load.
- High-voltage load.
- Primary energy storage element.
- Resistors for source level setting.

#### Three-way screw terminals

- Energy storage element (Battery or (super)capacitor).

#### 2-pin "Shrouded Header"

- Alternative connection for the storage element.

#### 3-pin headers

- Source level range configuration.
- Low drop-out regulators (LDOs) enabling.
- Energy storage elements and LDOs configuration.
- Dual-cell supercapacitor configuration.
- AC rectifier selection.
- Source level measurement enabling.

#### 2-pin headers

- Primary battery configuration.
- Connection of the on-board potentiometer for source level setting.

#### Provision for resistors

- Source level configuration.
- Custom mode configuration.
- Primary battery configuration.

#### 1-pin headers

- Access to status pins.

### EvB Information

Part Number	Dimensions
2AAEM00941C001 REV:2	76 mm x 49 mm

### Device Information

Part Number	Dimensions
10AEM00941C0000	4 mm x 4 mm

# 1. Connections Diagram

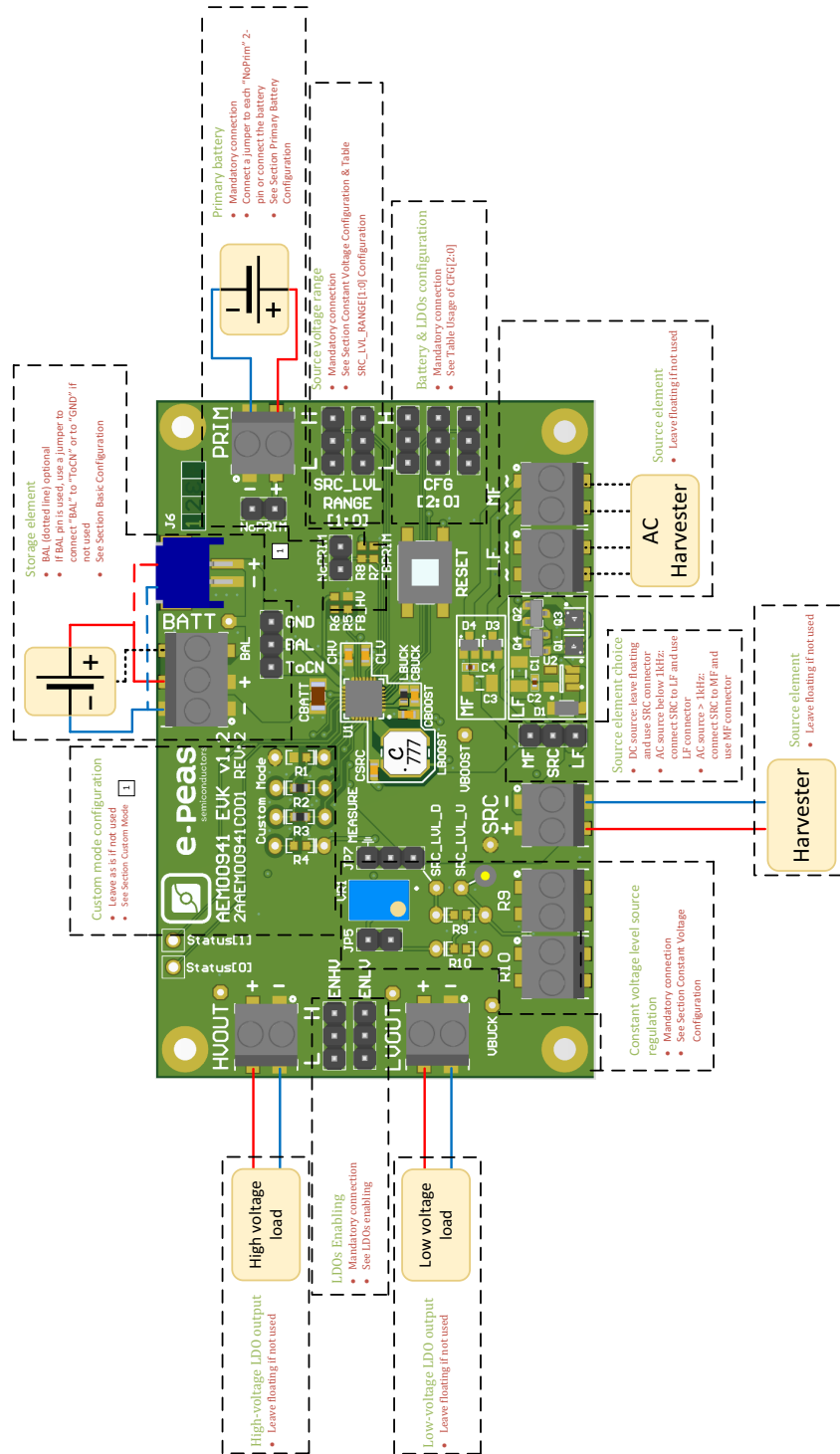


Figure 1: Connection Diagram

**NOTE:** if R1, R2, R3, R4 and R20 are not mounted (and thus *SET\_OVDIS*, *SET\_OVCH* and *SET\_CHRDY* are floating), make sure that no power source is connected to *SRC* or to *PRIM* when *CFG[2:0]* is LLL (custom mode) or floating. This would lead to damaging the AEM00941. Having *SET\_OVDIS*, *SET\_OVCH* and *SET\_CHRDY* tied to *BUCK* by installing 0 Ω on R2, R3 and R20 prevents this behavior.

## 1.1. Signals Description

		If used	If not used
NAME	FUNCTION	CONNECTION	
<b>Power signals</b>			
SRC	Connection to the harvested energy source.	Connect the source element.	
BATT	Connection to the energy storage element.	Connect the storage element in addition to CBATT <sup>1</sup> (min 150 µF).	Do not remove CBATT.
BAL	Connection to mid-point of a dual-cell supercapacitor.	Connect mid-point of supercapacitor and a jumper from "BAL" to "ToCN".	Use a jumper to connect "BAL" to "GND".
PRIM	Connection to the primary battery.	Connect primary battery and remove the "NoPRIM" jumpers.	Connect a jumper to each "NoPRIM" 2-pin.
LVOUT	Output of the low-voltage LDO regulator.	Connect a load.	Leave floating
HVOUT	Output of the high-voltage LDO regulator.	Connect a load.	Leave floating
LF	Connection to the AC harvested energy source (low frequency).	Connect to the source element.	Leave floating.
MF	Connection to the AC harvested energy source (medium frequency).	Connect to the source element.	Leave floating.
<b>Debug signals</b>			
VBOOST	Output of the boost converter.		
VBUCK	Output of the buck converter.		
BUFSRC	Connection to an external capacitor buffering the boost converter input.		
<b>Configuration signals</b>			
CFG[2:0]	Configuration of the threshold voltages for the energy storage element.	Connect jumpers (see Table 2).	Cannot be left floating (see Table 2).
SRC_LVL_RANGE[1:0]	Constant voltage harvesting range multiplier.	Connect jumpers (see Table 4).	Cannot be left floating (see Table 4).
SRC_LVL_D SRC_LVL_U	Constant voltage harvesting range.	Three alternatives (see Section 2.3.2): <ul style="list-style-type: none"> <li>- Use the potentiometer VR1 by placing a jumper on JP5, and another jumper between the middle pin and the pin below it on JP7.</li> <li>- Connect resistors on R9-R10 connectors.</li> <li>- Solder resistors on R9-R10 footprints.</li> </ul>	Cannot be left floating (see Section 2.3.2).
FB_PRIM_D FB_PRIM_U	Configuration of the primary battery.	Use resistors R7-R8 (see Section 2.3.3).	Connect a jumper to each "NoPRIM" 2-pin.
FB_HV	Configuration of the high-voltage LDO in the custom mode.	Use resistor R5-R6 (see Section 2.3.1).	Leave floating.
<b>Control signals</b>			
ENHV	Enabling pin for the high-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating.
ENLV	Enabling pin for the low-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating.
<b>Status signals</b>			
STATUS[1]	Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.		
STATUS[0]	Logic output. Asserted when the LDOs can be enabled.		

Table 1: Pin Description

1. CBATT capacity on the EvK may vary depending on suppliers availability, with a minimum value of 150µF.

## 2. General Considerations

### 2.1. Safety Information

Always connect the elements in the following order:

1. Reset the board - see “How to reset the AEM00941 evaluation board” on Figure 2.
  2. Completely configure the PCB (jumpers/resistors):
    - Source level configuration (SRC\_LVL\_RANGE[1:0]) -Table 4.
    - Battery and LDOs configuration (CFG[2:0] and, if needed, R1 to R6) - see Table 2.
    - Primary battery configuration (“NoPRIM” or R7-R8) - see Section 2.3.3.
    - LDOs enabling (ENHV and ENLV) - see Table 3.
    - Balancing circuit connection (BAL) - see Section 2.3.4.
  3. Connect the storage elements on BATT and optionally the primary battery on PRIM.
  4. Connect the high and/or low voltage loads on HVOUT/LVOUT (optional).
  5. Connect the Low or High frequency source on AC or DC SRC. Do not use both simultaneously.
- To avoid damage to the board, users are urged to follow this procedure.

How to reset the AEM00941 evaluation board:

To reset the board, simply disconnect the storage element and the optional primary battery and press the reset button in order to discharge the internal nodes of the system.

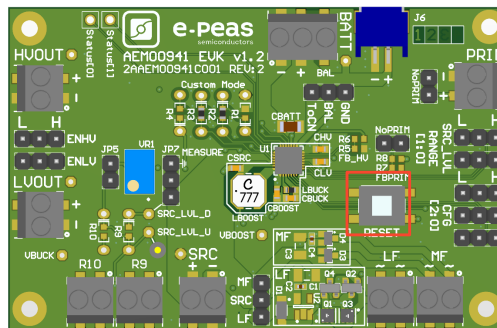


Figure 2: Board Reset

### 2.2. Basic Configurations

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V <sub>OVCH</sub>	V <sub>CHRDY</sub>	V <sub>OVDIS</sub>	V <sub>HV</sub>	V <sub>LV</sub>	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode - see Section 2.3.1.				1.8 V	

Table 2: Usage of CFG[2:0]

ENLV	ENHV	LV output	HV output
H	H	Enabled	Enabled
H	L	Enabled	Disabled
L	H	Disabled	Enabled
L	L	Disabled	Disabled

Table 3: LDOs enabling

## 2.3. Advanced Configurations

A complete description of the system constraints and configurations is available in the AEM00941 datasheet “System configuration” Section.

A reminder on how to calculate the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found on e-peas website.

### 2.3.1. Custom Mode

In addition to the pre-defined storage element protection levels, the custom mode allows users to define their own levels via resistors R1 to R4 and to tune the output of the high voltage LDO **HVOUT** via resistors R5-R6.

Here is how to determine the values of R1-R4 to set the desired storage element protection levels:

- $R_T = R_1 + R_2 + R_3 + R_4$
- $1\text{M}\Omega \leq R_T \leq 100\text{M}\Omega$
- $R_1 = R_T \cdot \frac{1\text{V}}{V_{\text{OVCH}}}$
- $R_2 = R_T \cdot \left( \frac{1\text{V}}{V_{\text{CHR DY}}} - \frac{1\text{V}}{V_{\text{OVCH}}} \right)$
- $R_3 = R_T \cdot \left( \frac{1\text{V}}{V_{\text{OV DIS}}} - \frac{1\text{V}}{V_{\text{CHR DY}}} \right)$
- $R_4 = R_T \cdot \left( 1 - \frac{1\text{V}}{V_{\text{OV DIS}}} \right)$

Here is how to determine the values of R5-R6 to set the desired **HVOUT** voltages:

- $R_V = R_5 + R_6$
- $1\text{M}\Omega \leq R_V \leq 40\text{M}\Omega$
- $R_5 = R_V \cdot \frac{1\text{V}}{V_{\text{HV}}}$
- $R_6 = R_V \cdot \left( 1 - \frac{1\text{V}}{V_{\text{HV}}} \right)$

Make sure the protection levels satisfy the following conditions:

- $V_{\text{CHR DY}} + 0.05\text{V} \leq V_{\text{OVCH}} \leq 4.5\text{V}$

Configuration pins		
<b>SRC_LVL_RANGE[1:0]</b>	Gain	$V_{\text{SRC\_REG}}$ range
LL	x1	$V_{\text{SRC\_REG}} < 1.35\text{V}$
LH	x2	$1.35\text{V} < V_{\text{SRC\_REG}} < 2.70\text{V}$
HL	x4	$2.70\text{V} < V_{\text{SRC\_REG}} < 4.47\text{V}$
HH		

Table 4: SRC\_LVL\_RANGE[1:0] Configuration

- $V_{\text{OV DIS}} + 0.05\text{V} \leq V_{\text{CHR DY}} \leq V_{\text{OVCH}} - 0.5\text{V}$
- $2.2\text{V} \leq V_{\text{OV DIS}}$
- $V_{\text{HV}} \leq V_{\text{OV DIS}} - 0.3\text{V}$

If custom mode used:

- Remove R2, R3 and R20 zero ohm resistors.
- Set resistors R1 to R6 to configure the custom mode.

If custom mode unused:

- Leave the resistor footprints of R1 to R6 empty.
- Place 0 ohm resistors on R20.
- Do not set **CFG[2:0]** to LLL.

### 2.3.2. Constant Voltage Configuration

The regulated harvesting voltage  $V_{\text{SRC\_REG}}$  can be defined by the use of the resistors R9 and R10.

**SRC\_LVL\_RANGE[1:0]** must be set according to the range of  $V_{\text{SRC\_REG}}$  as shown in Table 4 by using the following formulas:

- $R_S = R_9 + R_{10}$
- $100\text{k}\Omega \leq R_S \leq 1\text{M}\Omega$
- $R_9 = \frac{V_{\text{SRC\_REG}}}{\text{Gain}} \cdot R_S \cdot \frac{1}{2.2\text{V}}$
- $R_{10} = R_S - R_9$

R9 and R10 must either be set by:

- Soldering SMD/through-hole resistors on the R9-R10 footprints.
- Inserting through-hole resistors in the R9-R10 connectors.
- Using the EVK 200 kΩ potentiometer VR1 which is connected to **VBUCK** through R19 (100 kΩ).

The procedure of setting  $V_{\text{SRC\_REG}}$  through VR1 is the following:

- Ensure that neither of R9 and R10 are installed on either the footprints or the screw connectors.
- Place a jumper on JP5.

- Make sure the AEM00941 has coldstarted and that **VBUCK** is 2.2 V. The power available on **SRC** must be larger than 100  $\mu$ W.
- Connect a jumper on JP7 between the middle pin and the pin above it to ensure that the resistive divider (VR1 and R19) is always grounded.
- Connect a voltmeter between **GND** and **SRC\_LVL\_U** using the dedicated test point below VR1.
- $V_{\text{SRC,REG}} = \text{Gain} \cdot \text{SRC\_LVL\_U}$
- Move the jumper on JP7 to connect the middle pin and the pin below it.
- Remove the voltmeter and test with a source connected on **SRC**.

*NOTE: If the potentiometer VR1 is not used to configure the source constant voltage, please leave JP5 and JP7 without jumpers.*

### 2.3.3. Primary Battery Configuration

If a primary storage is used, it is mandatory to determine  $V_{\text{PRIM,MIN}}$ , the voltage at which the primary battery is considered fully depleted. To do so, use resistors R7 - R8.

These resistors are calculated as follows:

- $R_p = R7 + R8$
- $100\text{k}\Omega \leq R_p \leq 500\text{k}\Omega$
- $R7 = \frac{V_{\text{PRIM,MIN}}}{4} \cdot R_p \cdot \frac{1}{2.2\text{V}}$
- $R8 = R_p - R7$

If unused, use a jumper to short each “NoPRIM” 2-pin headers.

### 2.3.4. Balancing Circuit Configuration

When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balancing circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two supercapacitor cells to **BAL** (on **BATT** connector).
- Use a jumper to connect “**BAL**” to “**ToCN**”.

If unused, use a jumper to connect “**BAL**” to “**GND**”.

### 3. Functional Tests

This section presents a few simple tests that allow the user to understand the functional behavior of the AEM00941. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted make sure to properly reset the system to obtain reproducible results.

Those functional tests were made using the following setup:

- Configurations:
  - `SRC_LVL_RANGE[1:0] = LL`
  - `CFG[2:0] = HLL, ENHV = H, ENLV = H.`
- Storage element: Capacitor (4.7 mF + CBATT).
- Loads: 10 kΩ on `HVOUT`. `LVOUT` left floating.
- `SRC`: current source (1 mA or 100 μA) with voltage compliance (4V).

Feel free to adapt the setup to match your system as long as the input and cold-start constraints are respected (see the AEM00941 datasheet “Introduction” Section).

#### 3.1. Start-up

The following example allows users to observe the behavior of the AEM00941 in the wake-up mode.

##### Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.

##### Observations and Measurements

- `BATT`: Voltage rises as the power provided by the source is transferred to the storage element (see Figure 3).
- `SRC`: Regulated at  $V_{SRC\_REG}$ .
- `HVOUT/LVOUT`: Regulated when voltage on `BATT` first rises above  $V_{CHRDY}$  (see Figure 3).
- `STATUS[0]`: Asserted when the LDOs are ready to be enabled (refer to the AEM00941 datasheet “Normal Mode” section) (see Figure 3).

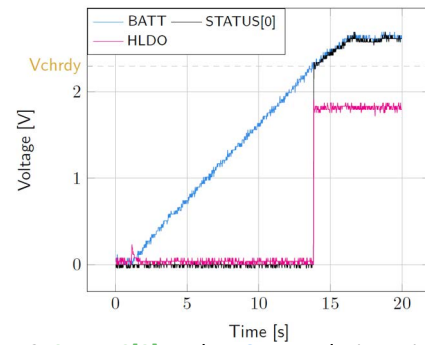


Figure 3: `STATUS[0]` and `HVOUT` evolution with `BATT`

#### 3.2. Shutdown

This test allows users to observe the behavior of the AEM00941 when the system is running out of energy.

##### Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1). Do not use a primary battery.
- Let the system reach a steady state (i.e. voltage on `BATT` between  $V_{CHRDY}$  and  $V_{OVCH}$  and `STATUS[0]` asserted).
- Remove the PV cell and let the system discharge through quiescent current and `HVOUT/LVOUT` load(s).

##### Observations and Measurements

- `BATT`: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage remains stable after crossing  $V_{OVDIS}$  (see Figure 4).
- `STATUS[0]`: De-asserted when the LDOs are no longer available as the storage element is running out of energy. This happens 600 ms after `STATUS[1]` assertion (see Figure 4).
- `STATUS[1]`: Asserted for 600ms when the storage element voltage (`BATT`) falls below  $V_{OVDIS}$  (see Figure 4).

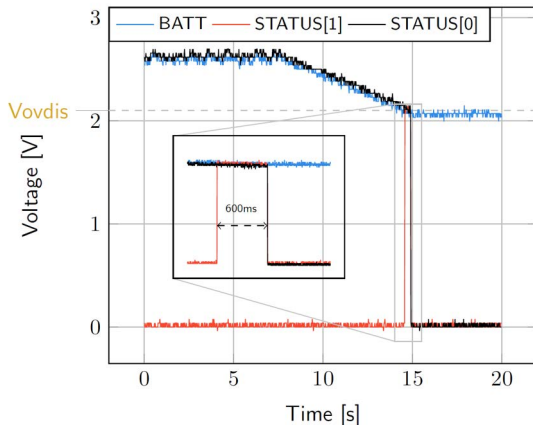


Figure 4: LDOs disabled around 600 ms after *BATT* reaches  $V_{OVDIS}$

### 3.3. Switching on Primary Battery

This example allows users to observe switching from the main storage element to the primary battery when the system is running out of energy.

#### Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1). Connect a primary battery (example: 3.1 V coin cell with protection level at 2.4 V,  $R7 = 68\text{ k}\Omega$  and  $R8 = 180\text{ k}\Omega$ ).
- Let the system reach a steady state (i.e. voltage on *BATT* between  $V_{CHRDY}$  and  $V_{OVDIS}$  and *STATUS[0]* asserted).
- Remove the PV cell and let the system discharge through quiescent current and *HVOUT/LVOUT* load(s).

#### Observations and Measurements

- *BATT*: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches  $V_{OVDIS}$  and then rises again to  $V_{CHRDY}$  as it is recharged from the primary battery (see Figure 5).

- *STATUS[0]*: Never de-asserted as the LDOs are still functional (see Figure 5).
- *HVOUT*: Stable and not affected by switching on the primary battery (see Figure 5).

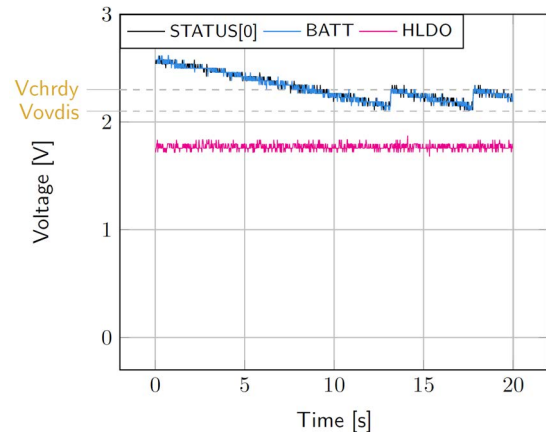


Figure 5: Switching from *SRC* to the primary battery

### 3.4. Cold Start

The following test allows the user to observe the minimum voltage required to coldstart the AEM00941. To prevent leakage current induced by the probe, the user should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behavior.

#### Setup

- Place the probes on the nodes to be observed.
- Referring Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Do not plug any storage element in addition to CBATT.
- *SRC*: Connect your source element.

#### Observations and Measurements

- *SRC*: Equal to the cold-start voltage during the cold-start phase. Regulated at the selected voltage when cold start is over. (See Figure 6). Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.
- *BATT*: Starts to charge when the cold-start phase is over (see Figure 6).



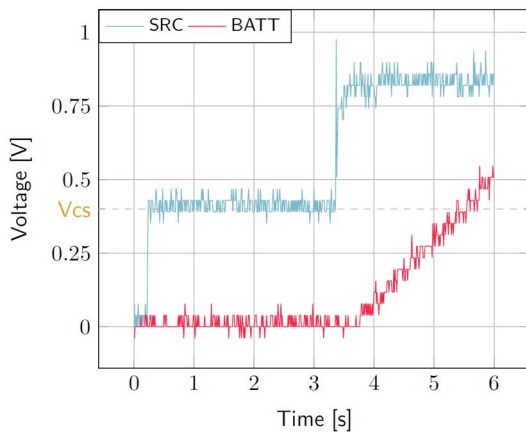


Figure 6: AEM00941 behavior during cold start

### 3.5. Dual-cell Supercapacitor Balancing Circuit

The following test allows the user to observe the balancing circuit behavior that balances the voltage on both side of the **BAL** pin.

#### Setup

- Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state. Plug the jumper linking “**BAL**” to “ToCN”.
- **BATT**: Plug a capacitor C1 between the positive (+) pin and the **BAL** pin, and a capacitor C2 between the **BAL** pin and the negative (-) pin.
  - $C1 \ \& \ C2 > 1 \text{ mF}$ .
  - $(C2 \times V_{\text{CHRDY}}) / C1 \geq 0.9 \text{ V}$ .
- **SRC**: Connect your source element to power up the system.

#### Observations and Measurements

- **BAL** voltage equals half of the **BATT** voltage.

**Warning regarding measurements:**

Any item connected to the PCB (load, probe, storage device, etc.) involves a leakage current. This can negatively impact the measurements. Whenever possible, disconnect unused items to limit this effect.

## 4. Performance Tests

This section presents the tests to reproduce the performance graphs found in the AEM00941 datasheet and to understand the functionalities of the AEM00941. To be able to reproduce those tests, the following equipment is required:

- 1 voltage source.
- 2 source measure units (SMUs).
- 1 oscilloscope.

To avoid damaging the board, follow the procedure in Section 2.1 “Safety Information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results (see “How to reset the AEM00941 evaluation board” in Section 2.1).

### 4.1. LDOs

The following example instructs users on how to measure the output voltage stability of the LDOs (Low-voltage and High-voltage LDO regulation Sections of the AEM00941 datasheet).

#### Setup

- Referring to Figure 1, follow steps 1 and 2 explained in the Section 2.1. Configure the board in the desired state and connect your storage element(s).
- **VBOOST**: Connect SMU1. Configure it to Voltage Source with a Current Compliance of 200 mA.
- **HVOUT** / **LVOUT**: Connect SMU2 to the LDO you want to measure. Configure it to sink current with a Voltage Compliance of 5 V for **HVOUT** or 2.5 V for **LVOUT**.

#### Manipulations

- Impose a voltage between  $V_{OVCH}$  and 5 V on SMU1 to force the AEM to start.
- Sweep voltage on SMU1 from  $V_{OVDIS} + 50$  mV to 4.5 V.
- Repeat with different current levels on SMU2 (from 10  $\mu$ A to 80 mA for **HVOUT** and from 10  $\mu$ A to 20 mA for **LVOUT**). Please make sure to set negative current values on SMU2 to simulate the load.

#### Measurements

- **HVOUT/LVOUT**: Measure the voltage.

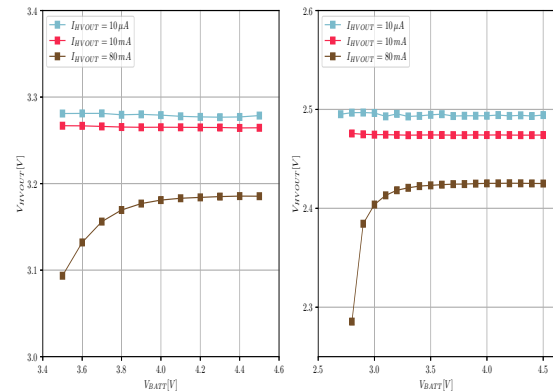


Figure 7: **HVOUT** at 3.3 V and 2.5 V

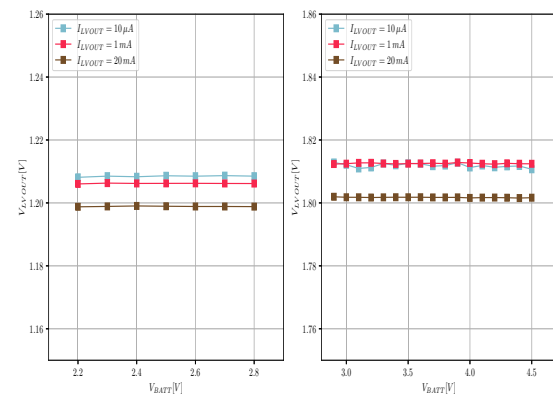


Figure 8: **LVOUT** at 1.2 V and 1.8 V

### 4.2. BOOST Efficiency

This test allows users to reproduce the efficiency graphs of the AEM00941 boost converter (Boost Conversion Efficiency Sections of the AEM00941 datasheet).

#### Setup

- Following steps 1 and 2 explained in the Section 2.1 and referring to Figure 1, configure the board in the desired state.
- **VBUCK**: Connect a 2.3 V Voltage Source to prevent **VBUCK** to sink current from **VBOOST**.
- **SRC**: Connect SMU1. Configure it to Current Source with a Voltage Compliance of 0 V.
- **VBOOST**: Connect SMU2 and configure it to Voltage Source with a Current Compliance of 200 mV.

### Manipulations

- Impose a voltage between  $V_{OVCH}$  and 5 V on SMU2 to force the AEM to start. When done, impose a voltage between  $V_{OVDIS} + 50$  mV and  $V_{OVCH}$ .
- Sweep voltage compliance on SMU1 from  $V_{OVDIS} + 50$  mV to 4.5 V.
- Repeat with different current levels on SMU1 (from 100  $\mu$ A to 10 mA) and with different voltage levels on SMU2 (from  $V_{OVDIS} + 50$  mV to  $V_{OVCH}$ ).

### Measurements

- **SRC**: Measure the current and the voltage.
- **VBOOST**: Measure the current and the voltage. Repeat the measurement a copious number of times to be sure to capture the current peaks. Figure 14 has been obtained by averaging over 100 measurements configured with a 100 ms integration time.
- Deduce input and output power ( $P = U \times I$ ) and efficiency ( $\eta = P_{out}/P_{in}$ ).

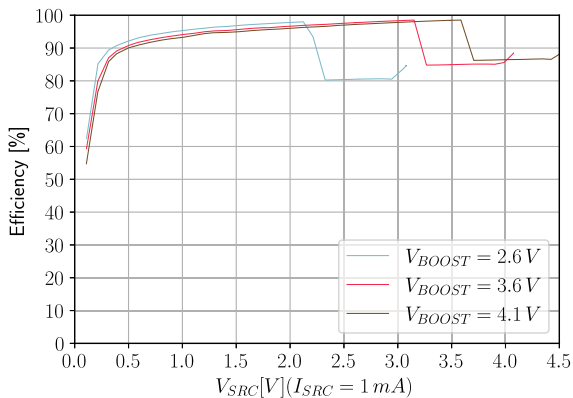


Figure 9: Boost efficiency for  $I_{SRC} = 1$  mA

## 4.3. Custom Mode Configuration

This test allows users to measure the custom protection levels of the storage element set by resistors R1 to R6.

### Setup

- Referring to Section 1, follow steps 1 and 2 explained in Section 2.1.
- To select custom mode:
  - Set  $CFG[2:0] = LLL$ .
  - Remove R2, R3 and R20.
  - Choose R1 to R6 to configure the battery protection levels and  $HVOUT$  output voltage.
- Place the probes on the nodes to be observed.
- **SRC**: connect your source element to power up the system.

### Manipulations

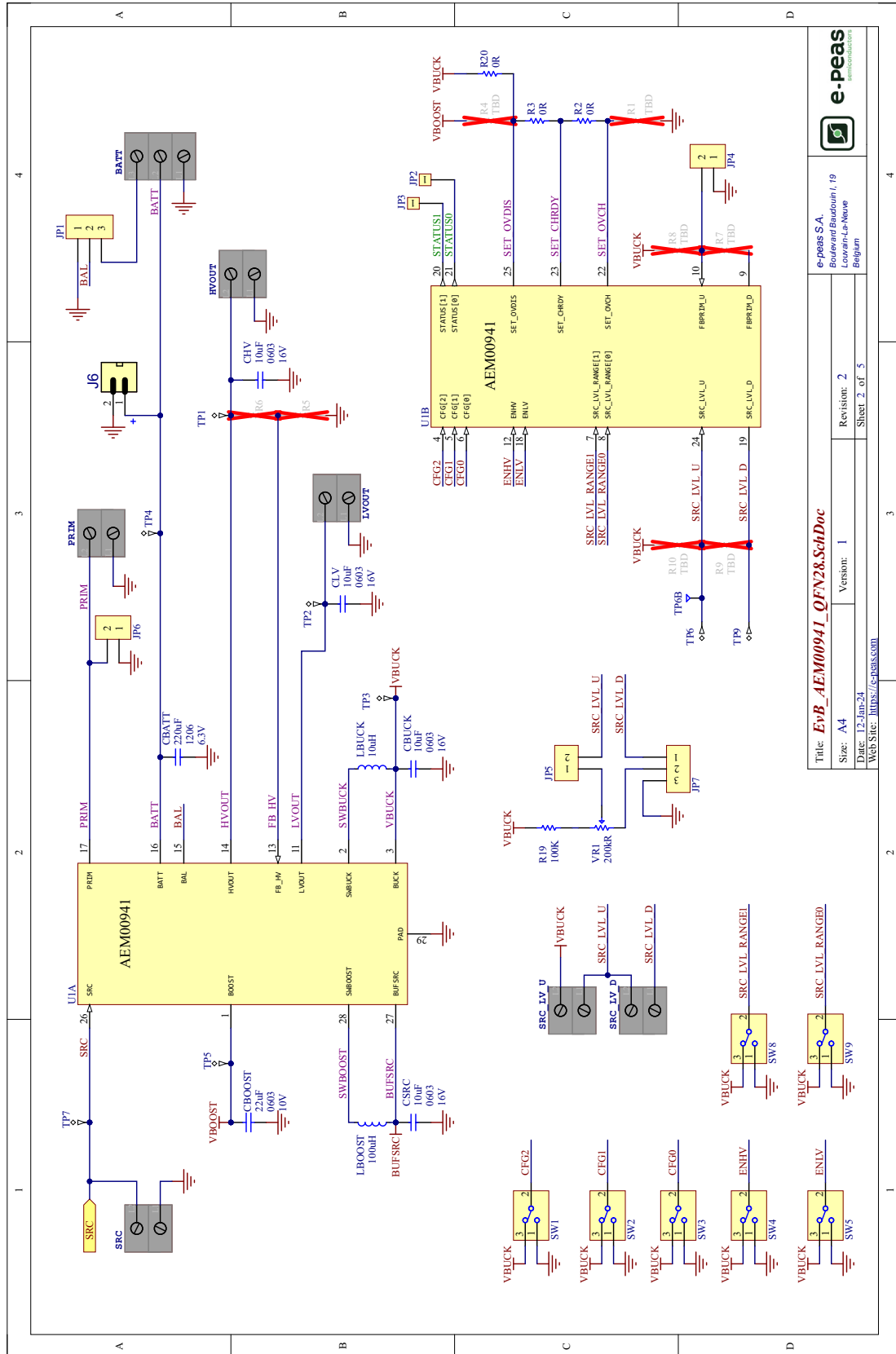
- Remove the source element after the voltage on **BATT** has reached steady state (between  $V_{CHRDY}$  and  $V_{OVCH}$ ).

### Measurements

Measure the following nodes to ensure the correct behavior of the AEM00941 with respect to the custom configuration:

- **STATUS[0]**: Asserted when the LDOs can be enabled (i.e. when **BATT** first rises above  $V_{CHRDY}$ ).
- **STATUS[1]**: Asserted when **BATT** falls below  $V_{OVDIS}$ .
- **BATT**: Rise up and oscillate around  $V_{OVCH}$  as long as the source element has not been removed.
- **HVOUT**: Equal to the value set by R5-R6.

## 5. Schematic



**e-peas SA**  
Boulevard Barthelemy, 19  
Louvain-la-Neuve  
Belgium

Title: **EVB\_AEM00941\_QFN28\_SchDoc**  
Size: A4  
Date: 12-Jan-24  
WebSite: <https://www.e-peas.com>

Version: 1  
Revision: 2  
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## 6. Revision History

EVK Version	User Guide Revision	Date	Description
1.1	1.0	October, 2023	Creation of the document
1.2	1.0	January, 2024	Update to EVK v1.2

Table 5: Revision history