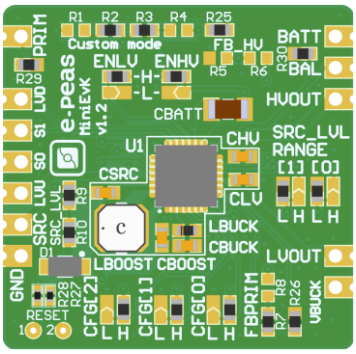
AEM00940
Quick Start Guide EVK



FEATURES

Pads

- 1 pad for the DC source
- 1 pad for the storage element
- 1 pad for primary battery
- 1 pad for HVOUT LDO output (80mA @ 1.8 – 4.1 V)
- 1 pad for LVOUT LDO output (20mA @ 1.2 or 1.8 V)

Configuration

- 2 solder pads SRC_LVL_RANGE[1:0] to define the input voltage regulation of the AEM
- 2 resistors to set the source voltage regulation
- 3 solder pads CFG[2:0] to define the storage element protection levels
- 6 resistors footprint related to the custom mode (CFG[000])
- 2 solder pads to enable/disable the internal LDOs
- 2 solder pads to disable the primary battery feature
- 1 solder pad to set the dual cell supercapacitor BAL feature

Size

- 28mm x 28mm

SUPPORT PCB

BOM around the AEM00940

Designator	Description	Quantity	Manufacturer	Part Number
U1	AEM0094x	1	e-peas	order at sales@e-peas.com
For AEM00940:				
L_{BOOST}	Power Inductor 10 µH - 0,55 A - LPS4012	1	Coilcraft	LPS4012-103MR
L_{BOOST} (alt.)	Power Inductor 10 µH - 0,84 A - 3015	1	Würth	744 040 321 00
L_{BOOST} (alt.)	Power Inductor 22 µH - 0,65 A - LPS4018	1	Coilcraft	LPS4018-223MR
For AEM00941:				
L_{BOOST}	Power Inductor 150 µH - 0,42 A - LPS5030	1	Coilcraft	LPS5030-154MRC
C_{BOOST}	Ceramic Cap 22 µF, 10 V, 20%, X5R, 0603	1	Murata	GRM188R61A226ME15D
L_{BUCK}	Power Inductor 10 µH - 0,25 A - 0603	1	TDK	MLZ1608M100WT
C_{BUCK}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{SRC}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{HV}	Ceramic Cap 10 µF, 25 V, 10%, X7S, 0805	1	TDK	C2012X7S1E106K125AE
C_{LV}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{BATT}	Ceramic Cap 150 µF, 6.3 V, 20%, X5R, 1206	1	TDK	GRM31CR60J157ME11L

Footprint & Symbol: Available in the datasheet

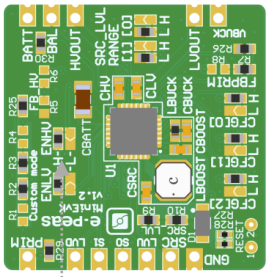
STEP 1: AEM00940 configuration

- **Source range:** SRC_LVL_RANGE[1:0]

Configuration pins		
SRC_LVL_RANGE[1:0]	Gain	V_{SRC_REG} range
LL	x1	V_{SRC_REG} < 1.35 V
LH	x2	1.35 V < V_{SRC_REG} < 2.70 V
HL	x4	2.70 V < V_{SRC_REG} < 4.47 V
HH		

- **Storage element voltages protection:** CFG[2:0]

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode				1.8 V	



- **BAL option:** Select “ToCn” to use the balancing or “GND” to disable it

- **PRIM option:** Leave R26 resistor to disable the primary battery feature or remove it if a primary battery is connected. Define the lower limit voltage on the primary battery using R7 and R8:

  - RP = R7 + R8
  - 100 kΩ ≤ RP ≤ 500 kΩ
  - R7 = $(\frac{Vprim\_min}{4}$ * RP) / 2.2 V
  - R8 = RP – R7

ENLV	ENHV	LV output	HV output
H	H	Enabled	Enabled
H	L	Enabled	Disabled
L	H	Disabled	Enabled
L	L	Disabled	Disabled

- **LDOs outputs voltages:** ENHV (HVOUT) – ENLV (LVOUT)

- **Source level:** Use the resistors R9 and R10 in combination of the source range functionality to define the harvesting voltage.

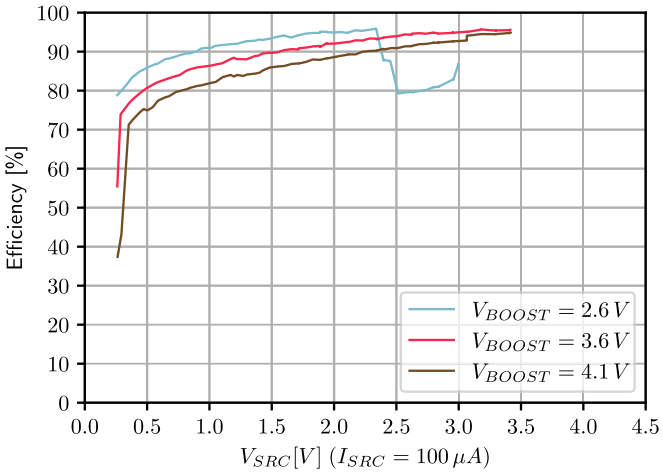
  - RS = R9 + R10
  - 100 kΩ ≤ RS ≤ 500 kΩ
  - R9 = $(\frac{Vsrc\_reg}{GAIN}$* RS) / 2.2 V
  - R10 = RS – R9

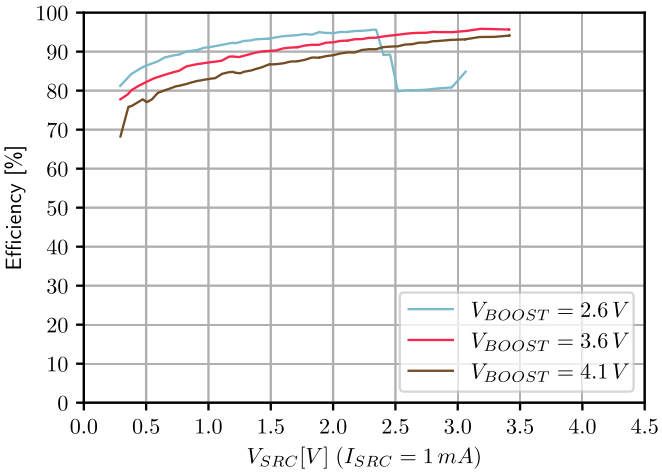
STEP 2: Connect the storage element (and the primary battery)

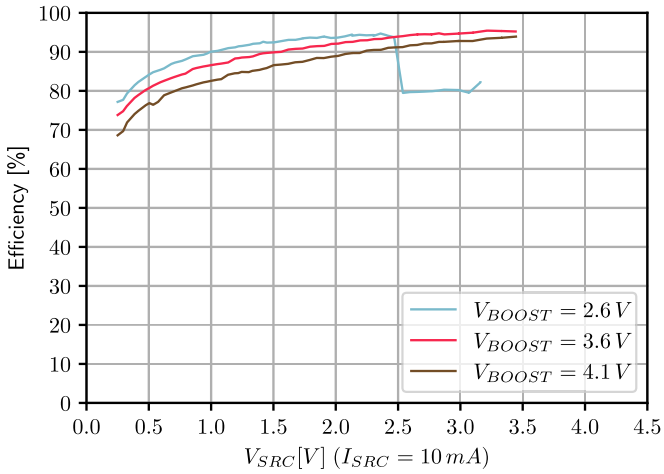
STEP 3: Connect the Load(s) to HVOUT / LVOUT

STEP 4: Connect the Harvester

Internal Boost efficiency Vs. input voltage 22µH LBOOST:







STEP 5: Check the Status

Status signals			
STATUS[1]	Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.		
STATUS[0]	Logic output. Asserted when the LDOs can be enabled.		