AEM00901 Stamp Module User Guide

Description

The AEM00901 Stamp Module is a printed circuit board (PCB) featuring all the required components to operate the AEM00901 integrated circuit (IC) in QFN28 package.

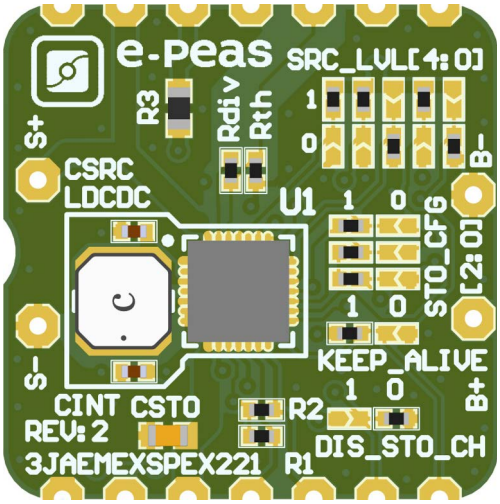
The AEM00901 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting or in product mock-ups.

It allows easy connections to an energy harvester (e.g. a single element PV cell) and a storage element. It also provides all the configuration access to set the device in any of the modes described in the datasheet at the exception of SRC_LVL_CFG[5], which has been tied to ground. The control and status signals are available on pads or through an I²C bus communication, allowing users to override preconfigured board settings through host MCU and evaluate the IC performances.

The AEM00901 Stamp Module is a plug and play, intuitive and efficient tool to optimize the AEM00901 configuration, allowing users to design a highly efficient subsystem for the desired target application. Component replacement and operating mode switching is convenient and easy.

More detailed information about AEM00901 features can be found in the datasheet.

Appearance



Features

Key features

- Very high efficiency conversion from single element PV.
- Very low BOM.
- Very small footprint.
- Ready to use without MCU interaction.
- Optional configuration through I²C.
- Thermal monitoring.

Breakout solder pads

- Connection to DC source of energy (PV).
- Connection to storage element.
- AEM Internal voltage.
- Temperature monitoring.
- Reset.
- I²C slave (address 0x41).
- Configuration.

Additional solder pads

- Connection to DC source of energy (PV).
- Connection to storage element.

Solder bridges and resistor

- Constant source voltage (SRC_LVL_CFG) configuration.
- Energy storage element threshold configuration.
- Mode configuration.

Applications

Wearable Electronics	Keyboards
Remote Control Units	Electronic Shelf Labels
Smart Buildings	Indoor Sensors

Evaluation Kit Information

Part Number	Dimensions
3JAEMEXSPEX221 REV:2	20 mm x 20 mm

Device Information

Part Number	Package	Body size
10AEM00900C0000	QFN 28-pin	4x4mm

1. Connections Diagram

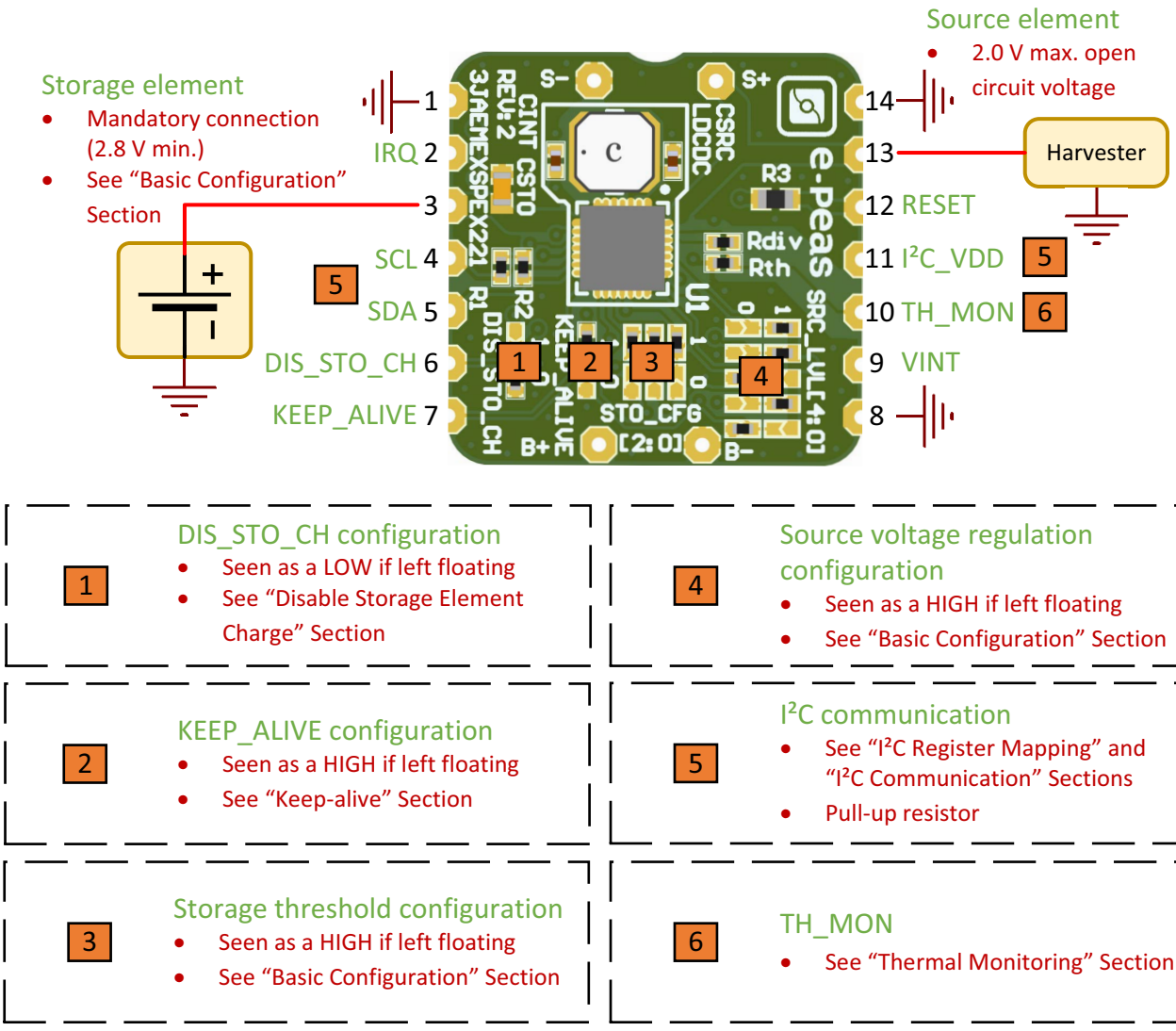


Figure 1: Connection diagram

2. Signals Description

NAME	FUNCTION	CONNECTION	
		If used	If not used
Power signals			
SRC	Connection to the harvested energy source.	Connect the source element.	Can be left floating.
STO	Connection to the energy storage element.	Cannot be left floating, voltage must always be above 2.5 V.	
I²C _VDD	Connection to I²C voltage supply.	Connect to I²C supply.	Connect to GND.
VINT	AEM Internal voltage supply.		

Table 1: Pin description

NAME	FUNCTION	CONNECTION	
		If used	If not used
BUFSRC	AEM connection to a capacitor buffering the boost converter input (no connector on EVK).		
Configuration signals			
SRC_LVL_CFG[5:0]	Used for the configuration of the source voltage level.	Connect solder bridges.	Read as HIGH if left floating.
STO_CFG[2:0]	Configuration of the threshold voltages for the energy storage element.	Connect solder bridges.	Read as HIGH if left floating.
TH_MON	Configuration of the thermal monitoring.	Connect a thermistor.	Connect to VINT.
Control signals			
DIS_STO_CH	Disabling pin for the storage charging.	Connect solder bridge (see Section 3.5.1).	Read as LOW if left floating.
KEEP_ALIVE	Enabling pin to supply internal circuitry from the storage element if no power on SRC.	Connect solder bridge (see Section 3.5.1).	Read as LOW if left floating.
I²C signals			
SDA	Bidirectional data line.	Connect to host I²C bus.	Connect I²C _VDD to GND (SDA and SCL will be pulled down by R_1 and R_2).
SCL	Unidirectional serial clock.		
IRQ	Interrupt request.	Connect to host GPIO.	Leave floating.

Table 1: Pin description

3. General Considerations

3.1. Safety Information

Always perform these steps in the following order:

1. Reset the board: do the following in this particular order:
   - Disconnect the harvester from SRC.
   - Short BUFSRC to GND.
   - Short VINT to GND.
2. Completely configure the PCB (resistors):
   - Source configuration.
   - Battery configuration.
   - Mode configuration.
   - Thermal monitoring configuration.
3. Connect I2C_VDD:
   - To GND if I²C is not used (SDA and SCL will also be connected to GND through their pull up resistors).
   - To a power supply if I²C is used (1.5 V to 5 V).
4. Connect the storage elements on STO with a voltage higher than 2.5 V.
5. Connect the source to the SRC connector (open circuit voltage lower than 3 V).

3.2. Basic Configurations

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0][a]						$V_{SRC,REG}$
L	L	L	H	H	L	0.12 V
L	L	L	H	H	H	0.13 V
L	L	H	L	L	L	0.15 V
L	L	H	L	L	H	0.16 V
L	L	H	L	H	L	0.18 V
L	L	H	L	H	H	0.19 V
L	L	H	H	L	L	0.21 V
L	L	H	H	L	H	0.22 V
L	L	H	H	H	L	0.24 V
L	L	H	H	H	H	0.25 V
L	H	L	L	L	L	0.27 V
L	H	L	L	L	H	0.28V
L	H	L	L	H	L	0.30 V
L	H	L	L	H	H	0.33 V
L	H	L	H	L	L	0.36 V
L	H	L	H	L	H	0.39 V
L	H	L	H	H	L	0.42 V
L	H	L	H	H	H	0.45 V
L	H	H	L	L	L	0.48 V
L	H	H	L	L	H	0.51 V
L	H	H	L	H	L	0.54 V
L	H	H	L	H	H	0.57 V
L	H	H	H	L	L	0.60 V
L	H	H	H	L	H	0.63 V
L	H	H	H	H	L	0.66 V
L	H	H	H	H	H	0.69 V

Table 2: Configuration of SRC_LVL_CFG[5:0]

a. On the AEM00901 stamp module, the MSB of the SRC_LVL_CFG[5:0] pins has been tied to ground (L).

Configuration	Configuration availability		Storage Element Threshold Voltage		Battery type
STO_CFG[2:0]	I²C Interface	Configuration pins	V_{OVCH}	V_{OVDIS}	
LLL	yes	yes	4.50 V	3.30 V	NiCd 3 cells
LLH	yes	yes	4.00 V	2.80 V	Tadrian TLI1020A
LHL	yes	yes	3.63 V	2.80 V	LiFePO4
LHH	yes	yes	3.90 V	2.80 V	Tadrian HCL1020
HLL	yes	yes	3.80 V	2.50 V	LIC
HLH	yes	yes	3.90 V	3.01 V	Li-ion (long life)
HHL	yes	yes	4.35 V	3.01V	LiPo
HHH	yes	yes	4.12 V	3.01 V	Li-ion/solid-state/ NiMH

Table 3: Usage of STO_CFG[2:0]

3.3. I²C Register Map

Address	Name	Bit	Field Name	Access	RESET	Description
0x00	VERSION	[7:0]	VERSION	R	-	Version number
0x01	SRCREGU	[6:0]	VALUE	R/W	0x77 (1.47V)	Source voltage regulation
0x02	VOVDIS	[5:0]	THRESH	R/W	0x2D (3.05V)	Overdischarge level of the storage element
0x03	VOVCH	[5:0]	THRESH	R/W	0x33 (4.1V)	Overcharge level of the storage element
0x04	TEMPCOLD	[7:0]	THRESH	R/W	0x8F (0°C)	Cold temperature level
0x05	TEMPHOT	[7:0]	THRESH	R/W	0x2F (45°C)	Hot temperature level
0x06	PWR	[0:0]	KEEPALEN	R/W	0x01	Keep-alive enable
		[1:1]	HPEN	R/W	0x01	High-power mode enable
		[2:2]	TMONEN	R/W	0x01	Temperature monitoring enable
		[3:3]	STOCHDIS	R/W	0x00	Battery charging disable
0x07	SLEEP	[0:0]	EN	R/W	0x01	Sleep mode enable
		[3:1]	THRESH	R/W	0x00	Sleep threshold
0x08	RSVD	[2:0]	-	R/W	-	This register can be written in but it will have no effect
0x09	APM	[0:0]	EN	R/W	0x00	APM enable
		[1:1]	RSVD1	R/W	0x00	Write 0x01 when APM is used.
		[3:2]	RSVD2	R/W	0x00	Write 0x00 when APM is used.
0x0A	IRQEN	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable
		[1:1]	VOVDIS	R/W	0x00	IRQ STO OVDIS enable
		[2:2]	VOVCH	R/W	0x00	IRQ STO OVCH enable
		[3:3]	SLPTHRESH	R/W	0x00	IRQ SRC LOW enable
		[4:4]	TEMP	R/W	0x00	IRQ temperature enable
		[5:5]	APMDONE	R/W	0x00	IRQ APM done enable
		[6:6]	APMERR	R	0x00	IRQ APM error enable
0x0B	CTRL	[0:0]	UPDATE	R/W	0x00	Load I²C registers configuration
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag
0x0C	IRQFLG	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag
		[1:1]	VOVDIS	R	0x00	IRQ STO OVDIS flag
		[2:2]	VOVCH	R	0x00	IRQ STO OVCH flag
		[3:3]	SLPTHRESH	R	0x00	IRQ SRC LOW flag
		[4:4]	TEMP	R	0x00	IRQ temperature flag
		[5:5]	APMDONE	R	0x00	IRQ APM done flag
		[6:6]	APMERR	R	0x00	IRQ APM error flag
0x0D	STATUS	[1:1]	VOVDIS	R	0x00	Status STO OVDIS
		[2:2]	VOVCH	R	0x00	Status STO OVCH
		[3:3]	SLPTHRESH	R	0x00	Status SRC LOW
		[4:4]	TEMP	R	0x00	Status temperature
		[6:6]	CHARGE	R	0x00	Status STO Charge
0x0E	APM0	[7:0]	DATA	R	0x00	APM data 0

Table 4: Register summary

Address	Name	Bit	Field Name	Access	RESET	Description
0x0F	APM1	[7:0]	DATA	R	0x00	APM data 1
0x10	APM2	[7:0]	DATA	R	0x00	APM data 2
0x11	TEMP	[7:0]	DATA	R	0x00	Temperature data
0x12	STO	[7:0]	DATA	R	0x00	Battery voltage
0x13		[7:0]		R		
0xE0	PN0	[7:0]	DATA	R	0X31	Part number 0 data
0xE1	PN1	[7:0]	DATA	R	0X30	Part number 1 data
0xE2	PN2	[7:0]	DATA	R	0X39	Part number 2 data
0xE3	PN3	[7:0]	DATA	R	0X30	Part number 3 data
0xE4	PN4	[7:0]	DATA	R	0X31	Part number 4 data

Table 4: Register summary

3.4. I²C Communication

The device address on the I²C bus is 0x41. All information about the I²C communication is available in the AEM00901 datasheet, “System configuration” Section.

I2C_VDD must be connected to an external power supply which voltage is within the 1.5 V to 2.2 V range. On the Stamp Module, 1 kΩ pull-up on SDA and SCL (R1 and R2) to I2C_VDD are provided.

In case one or more configurations are set by I²C communication, none of the configuration pins (GPIOs) will be taken into account anymore. Thus, applying the default values to any registers that have not been explicitly configured by I²C.

3.5. Advanced Configurations

A complete description of the system constraints and configurations is available in Section “System configuration” of the AEM00901 datasheet.

3.5.1. Mode Configuration

DIS_STO_CH

Enabling/disabling battery charging can be done by setting a solder bridge on the corresponding pad.

- Use a solder bridge to connect the DIS_STO_CH to H to disable the charge of the storage element.
- Use a solder bridge to connect the DIS_STO_CH to L to enable the charge of the storage element.

KEEP_ALIVE

The KEEP_ALIVE feature allows to supply the internal circuitry from the storage element when no power is available on the source terminal.

- Use a solder bridge to connect the KEEP_ALIVE to H to enable the feature.
- Use a solder bridge to connect the KEEP_ALIVE to L to disable the feature.

3.5.2. Thermal Monitoring

The thermal monitoring feature protects the battery by disabling the battery charging when ambient temperature is outside a specified range. The higher and lower thresholds are configurable using the I²C communication (see datasheet).

- Thermal monitoring is enabled by default on the Stamp Module. To disable it, users must connect “TH_MON” (pin 10, see Figure 1) to VINT (pin 9) externally.

4. Functional Tests

This section presents a few simple tests that allow users to understand the functional behavior of the AEM00901. To avoid damaging the board, follow the procedure found in Section 3.1. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results.

The measurements use the following equipment:

- Two Source Measurement Units (SMU, four-quadrant power supply).
- One 2-channel oscilloscope.

The following functional tests were made using the following setup:

- EVK jumpers configuration:
  - SRC_LVL_CFG[5:0] = HHLHL (0.54 V).
  - STO_CFG[2:0] = HHH (3.01 V - 4.12 V).
  - DIS_STO_CH = L.
  - KEEP_ALIVE = H.
- Place a jumper to connect I2C_VDD and GND if the I²C communication is not used.

Users can adapt the setup to match the use case system as long as the input limitations are respected, as well as the minimum storage voltage and cold-start constraints (see "Introduction" Section of AEM00901 datasheet).

4.1. Cold-start

The following test allows users to observe the minimum voltage required to coldstart the AEM00901. To prevent current leakage caused by the probe impedance, users should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behavior.

Setup

- Place oscilloscope probe on SRC.
- Referring Figure 1, follow steps 1 to 5 explained in Section 3.1.
- SRC: SMU set as 20 µA current source with 0.3 V voltage compliance.
- STO: SMU as 3.0 V voltage source with 100 µA current compliance.

Observations and measurements

- SRC voltage clamped at the cold-start voltage during the cold-start phase and then regulated at the selected $V_{SRC,REG}$ when cold start is over. The duration of the cold-start phase decreases as the input power increases. Select the input power accordingly to be able to observe the cold-start phase.
- STO: SMU starts absorbing current sourced by the STO pin once the cold-start phase is completed.

4.2. I²C Communication

This test allows users to change a configuration through the I²C communication.

Setup

- Place the oscilloscope probe on SRC.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 3.1. Configure theboard in the desired state and start the system.
- Connect I2C_VDD to the I²C supply (between 1.8 V and 5.5 V).
- Write '0010 0011' (0x23) on the register (0x01)
- Write '1' to the CTRL register (0x0B) to load the I²C register configuration (at startup the AEM00901 loads its configurations from the pins settings)

Observations and measurements

- SRC: observe that the voltage regulation switches to 0.285 V, when the register value is loaded

4.3. Efficiency

This test allows users to reproduce the efficiency graphs of the boost converter (see "DCDC Conversion Efficiency" Section in the AEM00901 datasheet.

Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 3.1. Configure the board in the desired state and start the system (see Section 3.1)
- STO: connect SMU configured as a 4.7 V voltage source with a 100 mA current compliance.
- SRC: connect SMU configured as a source current with a voltage compliance of 1.0 V to ensure the AEM00901 coldstarts.

Manipulations

- STO: set the SMU to the desired voltage, between V_{OVDIS} and V_{OVCH}. Make sure the SMU integration time is as long as possible.
- SRC: sweep the voltage compliance of the SMU from 0.12 V to 1.5 V to let the AEM00901 set VMPP according to the MPP ratio.

Observations and measurements

- For each data point of the SRC voltage sweep, note the SRC SMU voltage and current, as well as the STO SMU voltage and current. Repeat the measurement for each data point a copious number of times to ensure capturing current peaks.
- The efficiency η in percent is computed by applying the following formula:

$$\eta = 100 . \frac{V_{STO} \cdot I_{STO}}{V_{SRC} \cdot I_{SRC}}$$

5. DCDC Conversion Efficiency

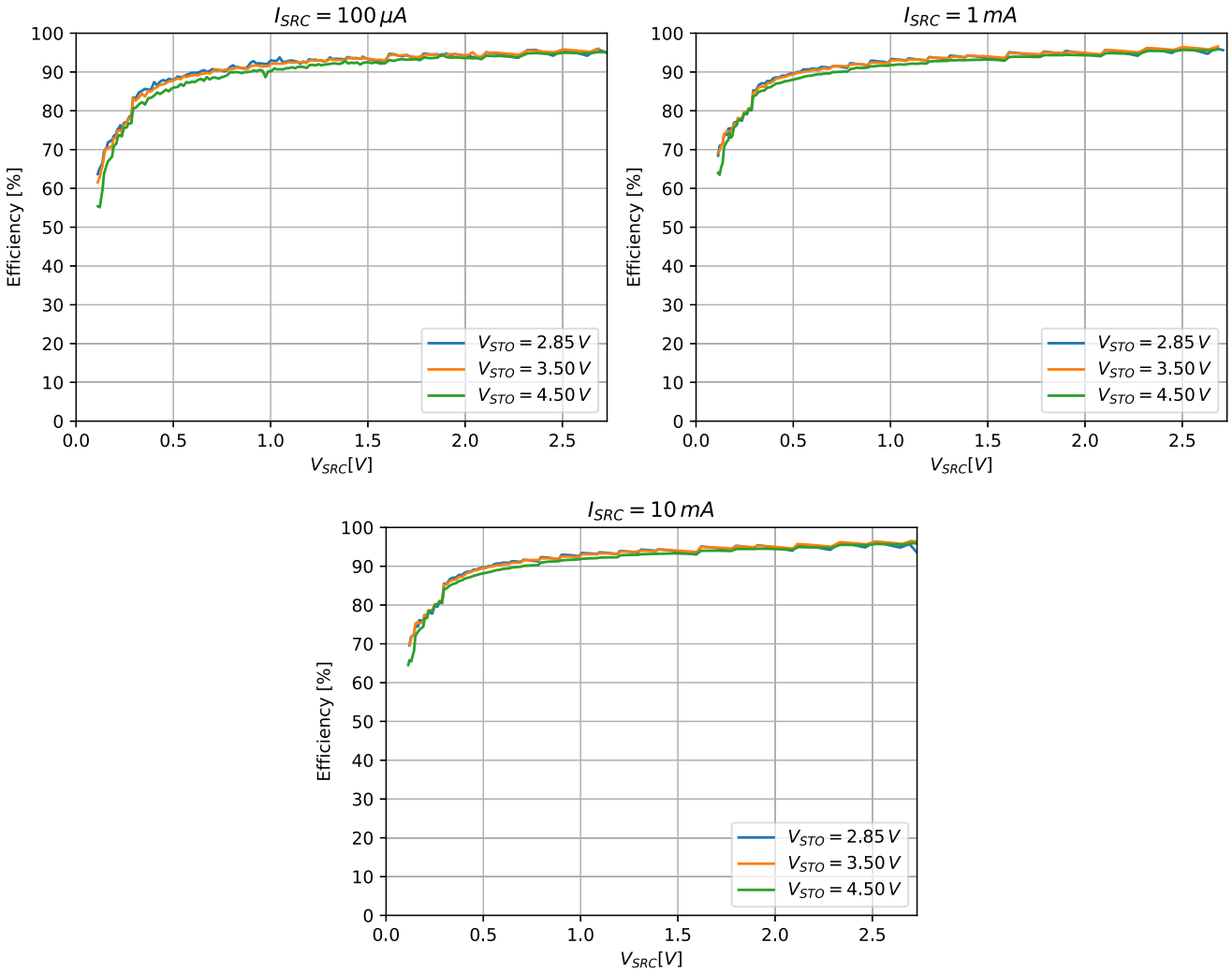


Figure 2: AEM00901 DCDC conversion efficiency (LDCDC: Coilcraft LPS4018-333MRB)

6. Schematics

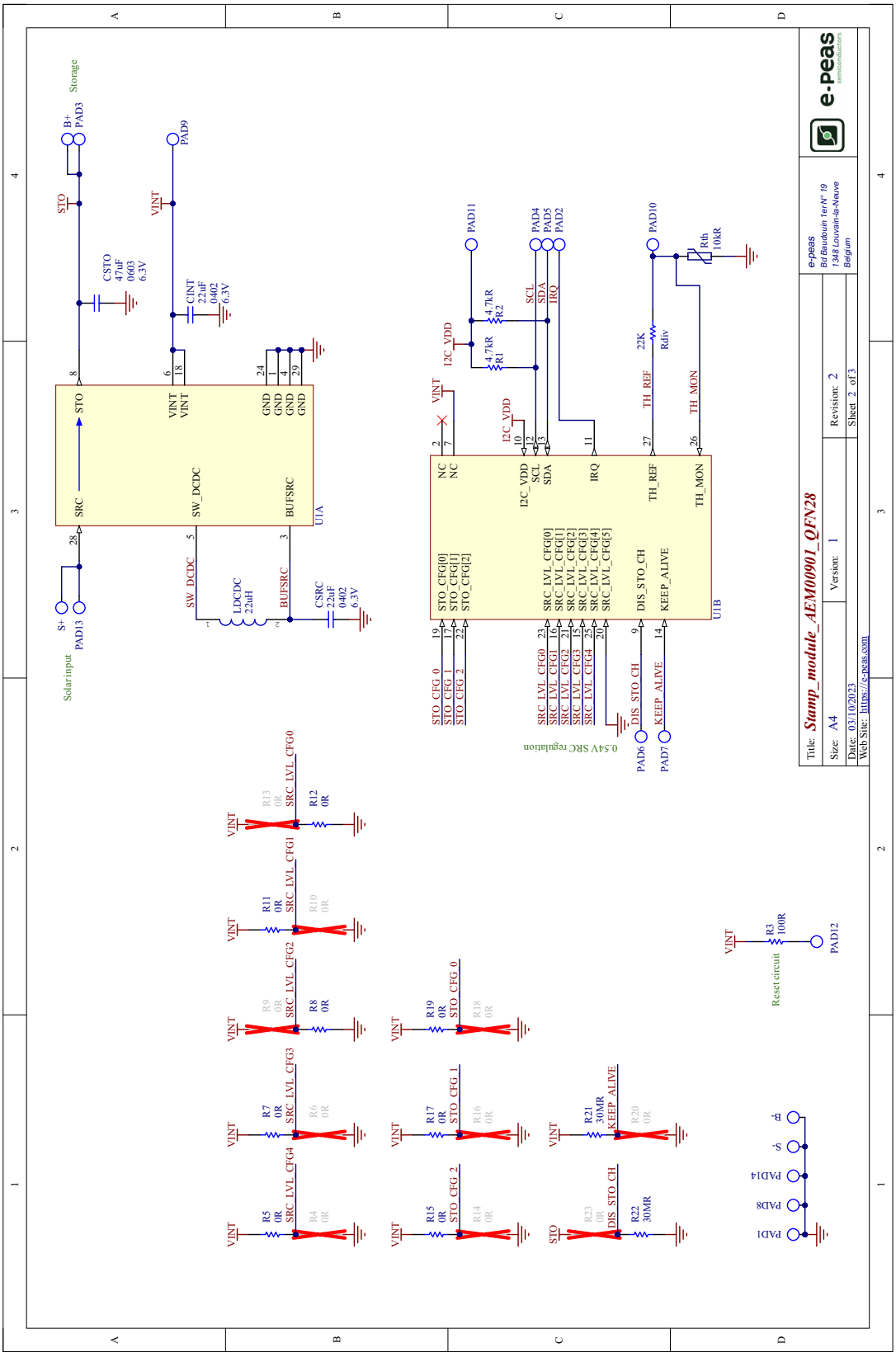


Figure 3: AEM00901 Stamp Module Schematic

7. Revision History

EVK Version	User Guide Revision	Date	Description
Up to 1.1	0.2	February, 2022	Creation of the document.
1.2	1.0	September, 2023	Fixed some inconsistencies and updated images.
1.2	1.1	August, 2024	Typos and aesthetic modifications throughout the document.

Table 5: Revision History